Datasheet

G32R501

Cortex-M52 Core-based 32-bit Real-time MCU

Version: V1.4

1. Product characteristics

Arm Cortex-M52 32-bit CPU (dual-core)

- 250 MHz
- IEEE 754 single-precision and double-precision floating point unit (FPU)
- Zidian Math Instruction Extension
  - Trigonometric math unit (TMU)
  - Viterbi/Complex mathematical unit (VCU)
- 8 hardware breakpoints
- Equipped with Helium™ technology based on vector extension scheme (MVE)

Memory

- 640KB embedded Flash (ECC protection)
- 128KB SRAM (parity protection)
- Support dual-zone security developed by third party
- Unique identification (UID) number

Clock and system control

- Two internal zero-pin 10MHz oscillators
- On-chip crystal oscillator and external clock input
- Window watchdog timer module
- Clock loss detection circuit

1.1V core, 3.3V I/O design

- Built-in 1.1V linear voltage regulator
- Brown-out reset (BOR) circuit

System peripherals

- 6-channel direct memory access (DMA) controller
- 44 independent programmable multiplexing general-purpose input/output (GPIO) pins
- Provide 31-channel digital inputs on the analog pins
- Enhanced external interrupt extension (EXTI) module
- Support multiple low-power modes (LPM) with external wake-up function

Communication peripherals

- 1 power management bus (PMBus) interface
- 1 internal integrated circuit (I2C) interface (pins are bootable)
- 2 controller area network (CAN) bus ports (pins are bootable)
- 2 serial peripheral interface (SPI) ports (pins are bootable)
- 2 serial communication interfaces (UART) (pins are bootable)
- 1 UART-compatible local interconnect network (LIN)
- 1 quad serial peripheral interface (QSPI)

Analog system

- 3 3.45 MSPS 12-bit analog-to-digital converters (ADC)
  - Up to 31 external channels
  - Each ADC has four integrated post-processing blocks (PPB)
- 7 window comparators (COMP) with 12-bit reference digital-to-analog converters (DAC)
  - Digital interference filter
- 2 12-bit buffer DAC outputs

Enhanced control peripherals

- 16 PWM channels with high-resolution function (150ps resolution)
  - Support of integrated dead zone with high resolution
  - Integrated hardware tripping zone (TZ)
- 7 enhanced capture (CAP) modules
  - Provide high-resolution capture (HRCAP) on 2 modules
- 2 enhanced quadrature encoder pulse (QEP) modules supporting CW/CCW operation modes

- 4 Σ-Δ sigma delta filter module (SDF) input channels (2 parallel filters per channel)
  - Standard SDF data filtering
  - The comparator filter is used to quickly perform operation in high or low-value situations

Flexible logic block (FLB)

- Enhance the functions of existing peripherals

Comply with the functional security standards

- Comply with IEC61508 SIL2 certification requirements

Related certifications

- AEC-Q100 Certification (certification is ongoing)
- IEC 61508 Certification (certification is ongoing)

Package options

- LQFP 100, 14mm*14mm
- LQFP 80, 12mm*12mm
- LQFP 80, 10mm*10mm
- LQFP 64, 10mm*10mm
- QFN 56, 7mm*7mm

Temperature option (ambient temperature)

- -40℃~105℃/125℃

Application

- Motor controller (servo/frequency converter/BLDC)
- On-board charger (OBC)
- DC power module for electric vehicle charging station
- Photovoltaic inverter (micro/string/central)
- Energy storage power conversion system (PCS)
- Three-phase UPS
- Industrial AC/DC power supply
- Commercial power supply (communication/server)

Contents

2. Product information

2.1. Product Information Table

See the following table for G32R5xx product functions and peripheral configuration.

Table 1 Functions and Peripherals of G32R5xx Series Chips

Product		G32R501				
Model Series		G32R501xCx7	G32R501xYx7	G32R501DxCx7	G32R501DxYx7	G32R501DxYx8Q
Model Configuration		Single-core/low-density	Single-core/high-density	Dual-core/low-density	Dual-core/high-density	Automotive/high-density
Processor and accelerator						
Series Type		Single-core		Single-core		Automotive (Dual-core)
CPU0：Cortex-M52	Frequency	250 MHz (TYP 200MHz)		250MHz (TYP 200MHz)		200 MHz
	FPU	Supported		Supported		Supported
	Zidian Computing Accelerator (VCU)	Supported		Supported		Supported
	Zidian Computing Accelerator (TMU)	Supported		Supported		Supported
CPU1：Cortex-M52	Frequency	-		250MHz (TYP 200MHz)		200 MHz
	FPU			Supported		Supported
	Zidian Computing Accelerator (VCU)			Supported		Supported
	Zidian Computing Accelerator (TMU)			Supported		Supported
6-Channel DMA		Supported				
Memory						
Series Type		Single-core		Single-core		Automotive (Dual-core)
		Low-density	High-density	Low-density	High-density	High-density
Flash total capacity (maximum)		256KB	640KB	256KB	640KB	640KB
CFGSMS (configurable memory array)	CPU0_ITCM	64KB	64KB	48KB	48KB	48KB
	CPU1_ITCM	-	-	8KB	8KB	8KB
	CPU0_DTCM	16KB	16KB	16KB	16KB	16KB
	CPU1_DTCM	-	-	8KB	8KB	8KB

Product		G32R501				
	SRAM1	8KB	8KB	8KB	8KB	8KB
	SRAM2	8KB	8KB	8KB	8KB	8KB
	SRAM3	32KB	32KB	32KB	32KB	32KB
	CFGSMS Total capacity (MAX)	128KB				
Flash ECC, on-chip memory parity protection, dual-zone security		Supported				
RAM Parity		Supported				
Boot ROM		128KB				
Configurable DCS OTP		8KB				
System						
Flexible logic block (FLB)		4 blocks				
32-bit CPU timer		3				
Watchdog timer		1				
Non-maskable interrupt watchdog (NMIWDT) timer		1				
Crystal oscillator/External clock input		1				
Zero-pin internal oscillator		2				
GPIO pin	QFN56	25				
	LQFP64	26				
	LQFP80	44				
	LQFP100	42				
AIO input	QFN56	14				
	LQFP64	16				
	LQFP80	16				
	LQFP100	31				
External Interrupt		16				
NVIC		226 (Max)				
Analog peripherals						
ADC 12-bit	Number	3				
	Million Samples Per Second (MSPS)	3.45				
	Conversion time (ns)	290				
	ADC channel	QFN56	14			
		LQFP64	16			

Product			G32R501
	(single-end)	LQFP80	16
		LQFP100	31
Temperature sensor			1
Buffer DAC			2
COMP		QFN56	6
		LQFP64	7
		LQFP80	7
		LQFP100	7
Control peripherals			
CAP/HRCAP			7 (2 with HRCAP function)
Channel of PWM/HRPWM			16
QEP			2
Channel of SDF		QFN56	2
		LQFP64	4
		LQFP80	2
		LQFP100	4
Communication peripherals			
CAN			2
I2C			1
UART			2
SPI			2
LIN (UART-compatible)			1
PMBus			1
QSPI			1
Voltage			
Operating voltage range			3.1V~3.6V
Temperature			
Junction temperature (TJ)			–40°C to 125℃/150°C
Ambient operating temperature (TA)			From -40° C to 105°C (xxx7 device model) From -40° C to 125°C (xxx8 device model)

2.2. Product model

For the product model configuration of G32R501, please refer to the table below.

Table 2 Device Model

Device model	Device package	Device configuration	AEC-Q100 Standard	Package code
G32R501DVYT7	LQFP100	Flash 640KB，RAM 128KB Dual-core/high-density	-	DVYT7
G32R501DMYT7	LQFP80			DMYT7
G32R501DPYT7	LQFP80			DPYT7
G32R501DRYT7	LQFP64			DRYT7
G32R501DNYU7	QFN56			DNYU7
G32R501VYT7	LQFP100	Flash 640KB，RAM 128KB Single-core/high-density	-	VYT7
G32R501MYT7	LQFP80			MYT7
G32R501RYT7	LQFP64			RYT7
G32R501NYU7	QFN56			NYU7
G32R501VCT7	LQFP100	Flash 256KB，RAM 128KB Single-core/low-density	-	VCT7
G32R501MCT7	LQFP80			MCT7
G32R501RCT7	LQFP64			RCT7
G32R501NCU7	QFN56			NCU7
G32R501DVCT7	LQFP100	Flash 256KB，RAM 128KB Dual-core/low-density	-	DVCT7
G32R501DMCT7	LQFP80			DMCT7
G32R501DRCT7	LQFP64			DRCT7
G32R501DNCU7	QFN56			DNCU7
G32R501DVYT8Q	LQFP100	Flash 640KB，RAM 128KB Automotive/high-density	Grade 1	DVYT8Q
G32R501DMYT8Q	LQFP80			DMYT8Q
G32R501DRYT8Q	LQFP64			DRYT8Q
G32R501DNYU8	QFN56	Flash 640KB，RAM 128KB Dual-core/ high-density /125℃ Ambient operating temperature	-	DNYU8

3. Pin information

3.1. Pin Definition Diagram

Figure 1 G32R5xx Series LQFP100 Pin Distribution Diagram

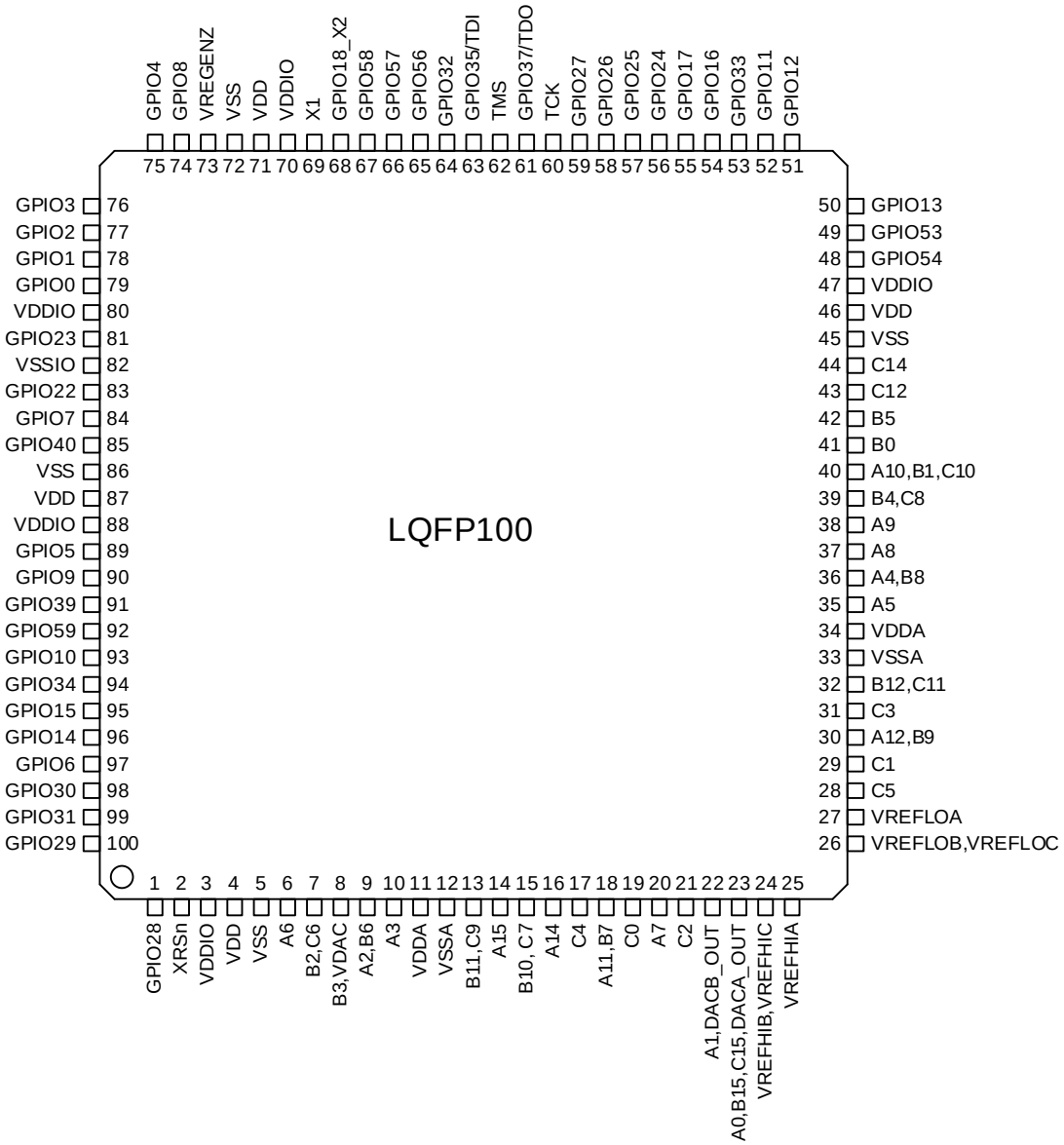


Figure 2 G32R5xx Series LQFP80 Pin Distribution Diagram

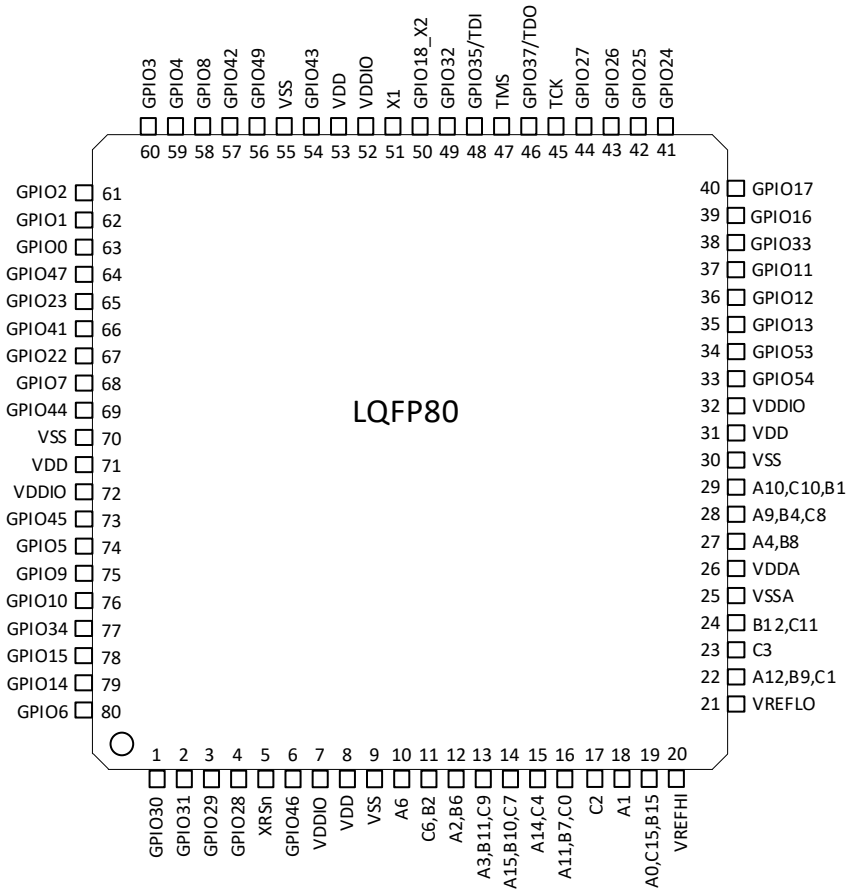


Figure 3 G32R5xx Series LQFP64 Pin Distribution Diagram

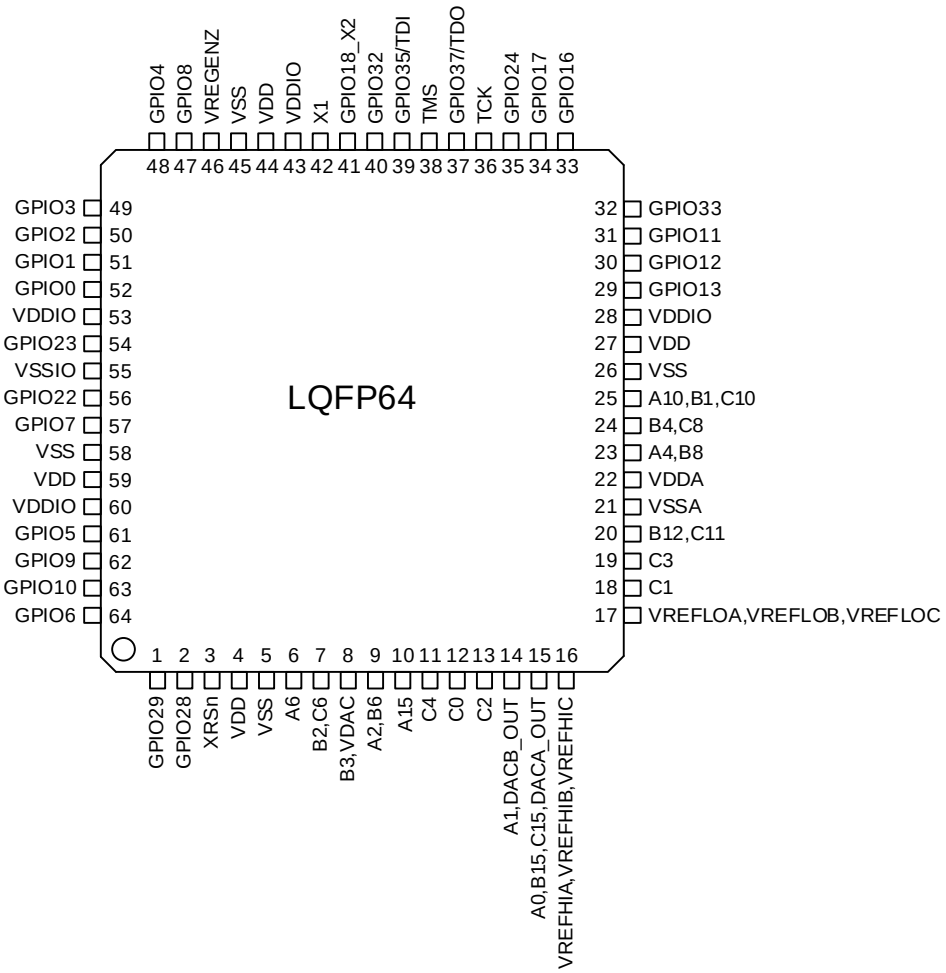
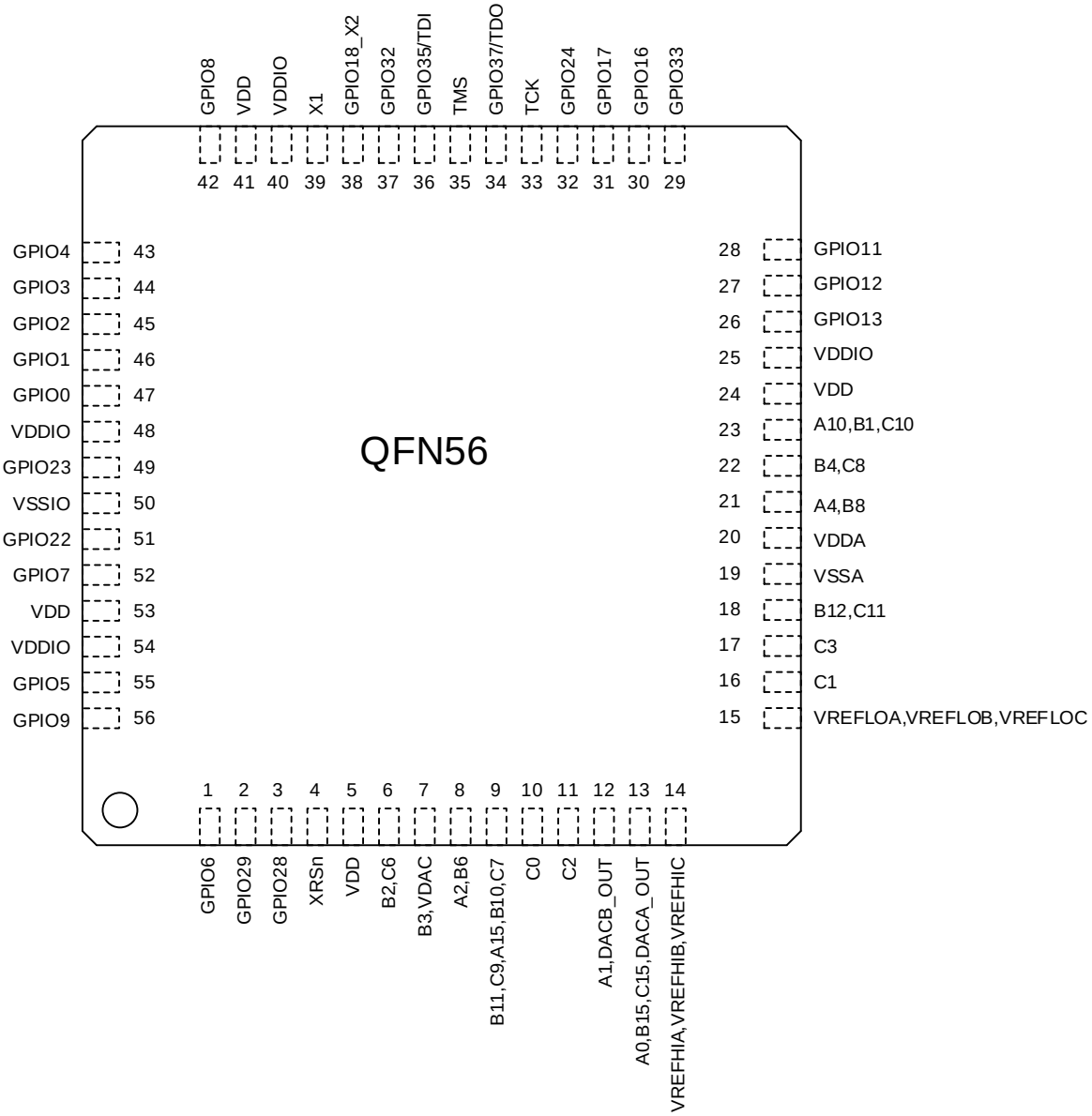


Figure 4 G32R5xx Series QFN56 Pin Distribution Diagram



3.2. Pin Attributes

Table 3 Pin Attributes

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
Analog							
A0		23	19	15	13	I	ADC-A Input 0
B15						I	ADC-B Input 15
C15						I	ADC-C Input 15
DACA_OUT						O	Buffer DAC-A Output
AIO231						I	Digital Input 231 on ADC Pin
A1		22	18	14	12	I	ADC-A Input 1
DACB_OUT						O	Buffer DAC-B Output
AIO232						I	Digital Input 232 on ADC Pin
A10		40	29	25	23	I	ADC-A Input 10
B1						I	ADC-B Input 1
C10						I	ADC-C Input 10
COMP7_HP0						I	COMP-7 High-level Comparator Positive Input 0
COMP7_LP0						I	COMP-7 Low-level Comparator Positive Input 0
AIO230						I	Digital Input 230 on ADC Pin
A2		9	12	9	8	I	ADC-A Input 2
B6						I	ADC-B Input 6
COMP1_HP0						I	COMP-1 High-level Comparator Positive Input 0

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
COMP1_LP0						I	COMP-1 Low-level Comparator Positive Input 0
AIO224						I	Digital Input 224 on ADC Pin
A3						I	ADC-A Input 3
COMP1_HP3						I	COMP-1 High-level Comparator Positive Input 3
COMP1_HN0		10	13	—	—	I	COMP-1 High-level Comparator Negative Input 0
COMP1_LP3						I	COMP-1 Low-level Comparator Positive Input 3
COMP1_LN0						I	COMP-1 Low-level Comparator Negative Input 0
AIO233						I	Digital Input 233 on ADC Pin
A4						I	ADC-A Input 4
B8						I	ADC-B Input 8
COMP2_HP0		36	27	23	21	I	COMP-2 High-level Comparator Positive Input 0
COMP2_LP0						I	COMP-2 Low-level Comparator Positive Input 0
AIO225						I	Digital Input 225 on ADC Pin
A5						I	ADC-A Input 5
COMP2_HP3						I	COMP-2 High-level Comparator Positive Input 3
COMP2_HN0		35	—	—	—	I	COMP-2 High-level Comparator Negative Input 0
COMP2_LP3						I	COMP-2 Low-level Comparator Positive Input 3
COMP2_LN0						I	COMP-2 Low-level Comparator Negative Input 0
AIO234						I	Digital Input 234 on ADC Pin
A6		6	10	6	—	I	ADC-A Input 6
COMP5_HP0						I	COMP-5 High-level Comparator Positive Input 0

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
COMP5_LP0						I	COMP-5 Low-level Comparator Positive Input 0
AIO228						I	Digital Input 228 on ADC Pin
A7		20	—	—	—	I	ADC-A Input 7
COMP5_HP3						I	COMP-5 High-level Comparator Positive Input 3
COMP5_HN0						I	COMP-5 High-level Comparator Negative Input 0
COMP5_LP3						I	COMP-5 Low-level Comparator Positive Input 3
COMP5_LN0						I	COMP-5 Low-level Comparator Negative Input 0
COMP3_HP2						I	COMP-3 High-level Comparator Positive Input 2
COMP3_LP2						I	COMP-3 Low-level Comparator Positive Input 2
AIO235						I	Digital Input 235 on ADC Pin
A8		37	—	—	—	I	ADC-A Input 8
COMP6_HP0						I	COMP-6 High-level Comparator Positive Input 0
COMP6_LP0						I	COMP-6 Low-level Comparator Positive Input 0
AIO229						I	Digital Input 229 on ADC Pin
A9		38	28	—	—	I	ADC-A Input 9
COMP6_HP3						I	COMP-6 High-level Comparator Positive Input 3
COMP6_HN0						I	COMP-6 High-level Comparator Negative Input 0
COMP6_LP3						I	COMP-6 Low-level Comparator Positive Input 3
COMP6_LN0						I	COMP-6 Low-level Comparator Negative Input 0
AIO236						I	Digital Input 236 on ADC Pin
A11		18	16	—	—	I	ADC-A Input 11

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
B7						I	ADC-B Input 7
COMP1_HP4						I	COMP-1 High-level Comparator Positive Input 4
COMP1_LP4						I	COMP-1 Low-level Comparator Positive Input 4
COMP1_HP2						I	COMP-1 High-level Comparator Positive Input 2
COMP1_LP2						I	COMP-1 Low-level Comparator Positive Input 2
AIO248						I	Digital Input 248 on ADC Pin
A12		30	22	—	—	I	ADC-A Input 12
B9						I	ADC-B Input 9
COMP2_HP4						I	COMP-2 High-level Comparator Positive Input 4
COMP2_LP4						I	COMP-2 Low-level Comparator Positive Input 4
COMP2_HP2						I	COMP-2 High-level Comparator Positive Input 2
COMP2_LP2						I	COMP-2 Low-level Comparator Positive Input 2
AIO249						I	Digital Input 249 on ADC Pin
A14		16	15	—	—	I	ADC-A Input 14
COMP5_HP4						I	COMP-5 High-level Comparator Positive Input 4
COMP5_LP4						I	COMP-5 Low-level Comparator Positive Input 4
COMP5_HP2						I	COMP-5 High-level Comparator Positive Input 2
COMP5_LP2						I	COMP-5 Low-level Comparator Positive Input 2
AIO252						I	Digital Input 252 on ADC Pin
A15		14	14	10	9	I	ADC-A Input 15
COMP6_HP4						I	COMP-6 High-level Comparator Positive Input 4

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
COMP6_LP4						I	COMP-6 Low-level Comparator Positive Input 4
AIO253						I	Digital Input 253 on ADC Pin
B0		41	—	—	—	I	ADC-B Input 0
COMP7_HP3						I	COMP-7 High-level Comparator Positive Input 3
COMP7_HN0						I	COMP-7 High-level Comparator Negative Input 0
COMP7_LP3						I	COMP-7 Low-level Comparator Positive Input 3
COMP7_LN0						I	COMP-7 Low-level Comparator Negative Input 0
AIO241						I	Digital Input 241 on ADC Pin
B2		7	11	7	6	I	ADC-B Input 2
C6						I	ADC-C Input 6
COMP3_HP0						I	COMP-3 High-level Comparator Positive Input 0
COMP3_LP0						I	COMP-3 Low-level Comparator Positive Input 0
AIO226						I	Digital Input 226 on ADC Pin
B3		8	—	8	7	I	ADC-B Input 3
VDAC						I	Optional External Reference Voltage for On-chip DAC. Please refer to the "Pin Signal Description" for precautions.
COMP3_HP3						I	COMP-3 High-level Comparator Positive Input 3
COMP3_HN0						I	COMP-3 High-level Comparator Negative Input 0
COMP3_LP3						I	COMP-3 Low-level Comparator Positive Input 3
COMP3_LN0						I	COMP-3 Low-level Comparator Negative Input 0
AIO242						I	Digital Input 242 on ADC Pin

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
B4		39	28	24	22	I	ADC-B Input 4
C8						I	ADC-C Input 8
COMP4_HP0						I	COMP-4 High-level Comparator Positive Input 0
COMP4_LP0						I	COMP-4 Low-level Comparator Positive Input 0
AIO227						I	Digital Input 227 on ADC Pin
B5		42	—	—	—	I	ADC-B Input 5
COMP4_HP3						I	COMP-4 High-level Comparator Positive Input 3
COMP4_HN0						I	COMP-4 High-level Comparator Negative Input 0
COMP4_LP3						I	COMP-4 Low-level Comparator Positive Input 3
COMP4_LN0						I	COMP-4 Low-level Comparator Negative Input 0
AIO243						I	Digital Input 243 on ADC Pin
B10		15	14	10	9	I	ADC-B Input 10
C7						I	ADC-C Input 7
COMP3_HP4						I	COMP-3 High-level Comparator Positive Input 4
COMP3_LP4						I	COMP-3 Low-level Comparator Positive Input 4
AIO250						I	Digital Input 250 on ADC Pin
B11		13	13	10	9	I	ADC-B Input 11
C9						I	ADC-C Input 9
COMP4_HP4						I	COMP-4 High-level Comparator Positive Input 4
COMP4_LP4						I	COMP-4 Low-level Comparator Positive Input 4
AIO251						I	Digital Input 251 on ADC Pin

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
B12		32	24	20	18	I	ADC-B Input 12
C11						I	ADC-C Input 11
COMP7_HP4						I	COMP-7 High-level Comparator Positive Input 4
COMP7_LP4						I	COMP-7 Low-level Comparator Positive Input 4
AIO254						I	Digital Input 254 on ADC Pin
C0		19	16	12	10	I	ADC-C Input 0
COMP1_HP1						I	COMP-1 High-level Comparator Positive Input 1
COMP1_HN1						I	COMP-1 High-level Comparator Negative Input 1
COMP1_LP1						I	COMP-1 Low-level Comparator Positive Input 1
COMP1_LN1						I	COMP-1 Low-level Comparator Negative Input 1
AIO237						I	Digital Input 237 on ADC Pin
C1		29	22	18	16	I	ADC-C Input 1
COMP2_HP1						I	COMP-2 High-level Comparator Positive Input 1
COMP2_HN1						I	COMP-2 High-level Comparator Negative Input 1
COMP2_LP1						I	COMP-2 Low-level Comparator Positive Input 1
COMP2_LN1						I	COMP-2 Low-level Comparator Negative Input 1
AIO238						I	Digital Input 238 on ADC Pin
C14		44	—	—	—	I	ADC-C Input 14
COMP7_HP1						I	COMP-7 High-level Comparator Positive Input 1
COMP7_HN1						I	COMP-7 High-level Comparator Negative Input 1
COMP7_LP1						I	COMP-7 Low-level Comparator Positive Input 1

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
COMP7_LN1						I	COMP-7 Low-level Comparator Negative Input 1
AIO246						I	Digital Input 246 on ADC Pin
C2		21	17	13	11	I	ADC-C Input 2
COMP3_HP1						I	COMP-3 High-level Comparator Positive Input 1
COMP3_HN1						I	COMP-3 High-level Comparator Negative Input 1
COMP3_LP1						I	COMP-3 Low-level Comparator Positive Input 1
COMP3_LN1						I	COMP-3 Low-level Comparator Negative Input 1
AIO244						I	Digital Input 244 on ADC Pin
C3		31	23	19	17	I	ADC-C Input 3
COMP4_HP1						I	COMP-4 High-level Comparator Positive Input 1
COMP4_HN1						I	COMP-4 High-level Comparator Negative Input 1
COMP4_LP1						I	COMP-4 Low-level Comparator Positive Input 1
COMP4_LN1						I	COMP-4 Low-level Comparator Negative Input 1
COMP4_HP2						I	COMP-4 High-level Comparator Positive Input 2
COMP4_LP2						I	COMP-4 Low-level Comparator Positive Input 2
AIO245						I	Digital Input 245 on ADC Pin
C4		17	15	11	—	I	ADC-C Input 4
COMP5_HP1						I	COMP-5 High-level Comparator Positive Input 1
COMP5_HN1						I	COMP-5 High-level Comparator Negative Input 1
COMP5_LP1						I	COMP-5 Low-level Comparator Positive Input1
COMP5_LN1						I	COMP-5 Low-level Comparator Negative Input 1

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
AIO239						I	Digital Input 239 on ADC Pin
C5		28	—	—	—	I	ADC-C Input 5
COMP6_HP1						I	COMP-6 High-level Comparator Positive Input 1
COMP6_HN1						I	COMP-6 High-level Comparator Negative Input 1
COMP6_LP1						I	COMP-6 Low-level Comparator Positive Input 1
COMP6_LN1						I	COMP-6 Low-level Comparator Negative Input 1
COMP6_HP2						I	COMP-6 High-level Comparator Positive Input 2
COMP6_LP2						I	COMP-6 Low-level Comparator Positive Input 2
AIO240						I	Digital Input 240 on ADC Pin
C12		43	—	—	—	I	ADC-C Input 12
COMP7_HP2						I	COMP-7 High-level Comparator Positive Input 2
COMP7_LP2						I	COMP-7 Low-level Comparator Positive Input 2
AIO247						I	Digital Input 247 on ADC Pin
VREFHIA		25	20	16	14	I/O	ADC-A High Reference Voltage. Please refer to the "Pin Signal Description" for precautions.
VREFHIB		24	20	16	14	I/O	ADC-B High Reference Voltage. Please refer to the "Pin Signal Description" for precautions.
VREFHIC		24	20	16	14	I/O	ADC-C High Reference Voltage. Please refer to the "Pin Signal Description" for precautions.
VREFLOA		27	21	17	15	I	ADC-A Low Reference Voltage. Please refer to the "Pin Signal Description" for precautions.
VREFLOB		26	21	17	15	I	ADC-B Low Reference Voltage. Please refer to the "Pin Signal Description" for precautions.

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
VREFLOC		26	21	17	15	I	ADC-C Low Reference Voltage. Please refer to the "Pin Signal Description" for precautions.
GPIO							
GPIO0	0, 4, 8, 12	79	63	52	47	I/O	General-Purpose Input/Output 0
PWM1_A	1					O	PWM-1 Output A
I2CA_SDA	6					I/OD	I2C-A Open-Drain Bidirectional Data
SPIA_STE	3					I/O	SPI-A Slave Transmit Enable
QSPI_IO1	11					I/O	QSPI_IO1
GPIO1	0, 4, 8, 12	78	62	51	46	I/O	General-Purpose Input/Output 1
PWM1_B	1					O	PWM-1 Output B
I2CA_SCL	6					I/OD	I2C-A Open-Drain Bidirectional Clock
SPIA_SOMI	3					I/O	SPI-A Slave Output, Master Input (SOMI)
GPIO2	0, 4, 8, 12	77	61	50	45	I/O	General-Purpose Input/Output 2
PWM2_A	1					O	PWM-2 Output A
OUTPUTXBAR1	5					O	Output X-BAR Output 1
PMBUSA_SDA	6					I/OD	PMBus-A Open-Drain Bidirectional Data
UARTA_TX	9					O	UART-A Transmit Data
QSPI_IO3	11					I/O	QSPI_IO3
SPIA_SIMO	3					I/O	SPI-A Slave Input, Master Output (SIMO)
CANA_TX	2					O	CAN-A Transmit
GPIO3	0, 4, 8, 12	76	60	49	44	I/O	General-Purpose Input/Output 3
PWM2_B	1					O	PWM-2 Output B

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
OUTPUTXBAR2	2, 5					O	Output X-BAR Output 2
CANA_RX	3					I	CAN-A Receive
PMBUSA_SCL	6					I/OD	PMBus-A Open-Drain Bidirectional Clock
SPIA_CLK	7					I/O	SPI-A Clock
UARTA_RX	9					I	UART-A Receive Data
QSPI_IO2	11					I	QSPI_IO2
GPIO4	0, 4, 8, 12	75	59	48	43	I/O	General-Purpose Input/Output 4
PWM3_A	1					O	PWM-3 Output A
OUTPUTXBAR3	5					O	Output X-BAR Output 3
CANA_TX	6					O	CAN-A Transmit
QSPI_SCLK	11					I/O	QSPI_SCLK
SPIB_CLK	3					I/O	SPI-B Clock
QEP2_STROBE	2					I	QEP-2 Gating
GPIO5	0, 4, 8, 12	89	74	61	55	I/O	General-Purpose Input/Output 5
PWM3_B	1					O	PWM-3 Output B
OUTPUTXBAR3	3					O	Output X-BAR Output 3
CANA_RX	6					I	CAN-A Receive
SPIA_STE	7					I/O	SPI-A Slave Transmit Enable (STE)
QSPI_IO1	11					I/O	QSPI_IO1
GPIO6	0, 4, 8, 12	97	80	64	1	I/O	General-Purpose Input/Output 6
PWM4_A	1					O	PWM-4 Output A

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
OUTPUTXBAR4	2					O	Output X-BAR Output 4
SYNCOUT	3					O	External PWM Synchronization Pulse
QEP1_A	5					I	QEP-1 Input A
CANB_TX	6					O	CAN-B Transmit
SPIB_SOMI	7					I/O	SPI-B Slave Output, Master Input (SOMI)
QSPI_IO0	11					I/O	QSPI_IO0
GPIO7	0, 4, 8, 12	84	68	57	52	I/O	General-Purpose Input/Output 7
PWM4_B	1					O	PWM-4 Output B
OUTPUTXBAR5	3					O	Output X-BAR Output 5
QEP1_B	5					I	QEP-1 Input B
CANB_RX	6					I	CAN-B Receive
SPIB_SIMO	7					I/O	SPI-B Slave Input, Master Output (SIMO)
QSPI_SS_N	11					I/O	QSPI_SS_N
GPIO8	0, 4, 8, 12	74	58	47	42	I/O	General-Purpose Input/Output 8
PWM5_A	1					O	PWM-5 Output A
CANB_TX	2					O	CAN-B Transmit
ADCSOCAO	3					O	ADC conversion start A signal output to external ADC (from PWM)
QEP1_STROBE	5					I/O	QEP-1 Gating
UARTA_TX	6					O	UART-A Transmit Data
SPIA_SIMO	7					I/O	SPI-A Slave Input, Master Output (SIMO)
I2CA_SCL	9					I/OD	I2C-A Open-Drain Bidirectional Clock

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
QSPI_IO3	11					I/O	QSPI_IO3
GPIO9	0, 4, 8, 12	90	75	62	56	I/O	General-Purpose Input/Output 9
PWM5_B	1					O	PWM-5 Output B
UARTB_TX	2					O	UART-B Transmit Data
OUTPUTXBAR6	3					O	Output X-BAR Output 6
QEP1_INDEX	5					I/O	QEP-1 index
UARTA_RX	6					I	UART-A Receive Data
SPIA_CLK	7					I/O	SPI-A Clock
QSPI_IO2	11					I/O	QSPI_IO2
GPIO10	0, 4, 8, 12	93	76	63		I/O	General-Purpose Input/Output 10
PWM6_A	1					O	PWM-6 Output A
CANB_RX	2					I	CAN-B Receive
ADCSOCBO	3					O	ADC conversion start B signal output to external ADC (from PWM)
QEP1_A	5					I	QEP-1 Input A
UARTB_TX	6					O	UART-B Transmit Data
SPIA_SOMI	7					I/O	SPI-A Slave Output, Master Input (SOMI)
I2CA_SDA	9					I/OD	I2C-A Open-Drain Bidirectional Data
QSPI_SCLK	11					I/O	QSPI_SCLK
GPIO11	0, 4, 8, 12	52	37	31	28	I/O	General-Purpose Input/Output 11
PWM6_B	1					O	PWM-6 Output B
UARTB_RX	2, 6					I	UART-B Receive data

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
OUTPUTXBAR7	3					O	Output X-BAR Output 7
QEP1_B	5					I	QEP-1 Input B
SPIA_STE	7					I/O	SPI-A Slave Transmit Enable (STE)
QSPI_IO1	11					I/O	QSPI_IO1
QEP2_A	10					I	QEP-2 Input A
SPIA_SIMO	13					I/O	SPI-A Slave Input, Master Output (SIMO)
GPIO12	0, 4, 8, 12	51	36	30	27	I/O	General-Purpose Input/Output 12
PWM7_A	1					O	PWM-7 Output A
CANB_TX	2					O	CAN-B Transmit
QEP1_STROBE	5					I/O	QEP-1 Gating
UARTB_TX	6					O	UART-B Transmit Data
PMBUSA_CTL	7					I	PMBus-A Control Signal
QSPI_IO0	11					I	QSPI_IO0
SPIA_CLK	3					I/O	SPI-A Clock
CANA_RX	10					I	CAN-A Receive
TRACED2	15					O	TRACE Synchronous Data Output 2
GPIO13	0, 4, 8, 12	50	35	29	26	I/O	General-Purpose Input/Output 13
PWM7_B	1					O	PWM-7 Output B
CANB_RX	2					I	CAN-B Receive
QEP1_INDEX	5					I/O	QEP-1 index
UARTB_RX	6					I	UART-B Receive data

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
PMBUSA_ALERT	7					I/OD	PMBus-A Open-Drain Bidirectional Alarm Signal
QSPI_SS_N	11					I/O	QSPI_SS_N
SPIA_SOMI	3					I/O	SPI-A Slave Output, Master Input (SOMI)
CANA_TX	10					O	CAN-A Transmit
TRACED3	15					O	TRACE Synchronous Data Output 3
GPIO14	0, 4, 8, 12	96	79	-	-	I/O	General-Purpose Input/Output 14
PWM8_A	1					O	PWM-8 Output A
UARTB_TX	2					O	UART-B Transmit Data
OUTPUTXBAR3	6					O	Output X-BAR Output 3
PMBUSA_SDA	7					I/OD	PMBus-A Open-Drain Bidirectional Data
SPIB_CLK	9					I/O	SPI-B Clock
QEP2_A	10					I	QEP-2 Input A
PWM3_A	5					O	PWM-3 Output A
GPIO15	0, 4, 8, 12	95	78	-	-	I/O	General-Purpose Input/Output 15
PWM8_B	1					O	PWM-8 Output B
UARTB_RX	2					I	UART-B Receive data
OUTPUTXBAR4	6					O	Output X-BAR Output 4
PMBUSA_SCL	7					I/OD	PMBus-A Open-Drain Bidirectional Clock
SPIB_STE	9					I/O	SPI-B Slave Transmit Enable (STE)
QEP2_B	10					I	QEP-2 Input B
PWM3_B	5					O	PWM-3 Output B

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
GPIO16	0, 4, 8, 12	54	39	33	30	I/O	General-Purpose Input/Output 16
SPIA_SIMO	1					I/O	SPI-A Slave Input, Master Output (SIMO)
CANB_TX	2					O	CAN-B Transmit
OUTPUTXBAR7	3					O	Output X-BAR Output 7
PWM5_A	5					O	PWM-5 Output A
UARTA_TX	6					O	UART-A Transmit Data
SD1_D1	7					I	SDF-1 Channel 1 Data Input
QEP1_STROBE	9					I/O	QEP-1 Gating
PMBUSA_SCL	10					I/OD	PMBus-A Open-Drain Bidirectional Clock
XCLKOUT	11					O	External Clock Output
QEP2_B	14					I	QEP-2 Input B
SPIB_SOMI	13					I/O	SPI-B Slave Output, Master Input (SOMI)
TRACED0	15					O	TRACE Synchronous Data Output 0
GPIO17	0, 4, 8, 12	55	40	34	31	I/O	General-Purpose Input/Output 17
SPIA_SOMI	1					I/O	SPI-A Slave Output, Master Input (SOMI)
CANB_RX	2					I	CAN-B Receive
OUTPUTXBAR8	3					O	Output X-BAR Output 8
PWM5_B	5					O	PWM-5 Output B
UARTA_RX	6					I	UART-A Receive Data
SD1_C1	7					I	SDF-1 Channel 1 Clock Input
QEP1_INDEX	9					I/O	QEP-1 index

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
PMBUSA_SDA	10					I/OD	PMBus-A Open-Drain Bidirectional Data
CANA_TX	13					O	CAN-A Transmit
TRGIO	15					I/O	External Trigger Bidirectional
GPIO18_X2	0, 4, 8, 12	68	50	41	38	I/O	General-Purpose Input/Output 18_X2. This pin and its digital multiplexer option can only be used when INTOSC is used as the system clock source and X1 is connected to an external pull-down resistor (1kΩ is recommended).
SPIA_CLK	1					I/O	SPI-A Clock
UARTB_TX	2					O	UART-B Transmit Data
CANA_RX	3					I	CAN-A Receive
PWM6_A	5					O	PWM-6 Output A
I2CA_SCL	6					I/OD	I2C-A Open-Drain Bidirectional Clock
SD1_D2	7					I	SDF-1 Channel 2 Data Input
QEP2_A	9					I	QEP-2 Input A
PMBUSA_CTL	10					I	PMBus-A Control Signal
XCLKOUT	11					O	External Clock Output
X2	ALT					O	Crystal Oscillator Output
GPIO20	0	—	—	—	—	I/O	General-Purpose Input/Output 20
QEP1_A	1					I	QEP-1 Input A
CANB_TX	3					O	CAN-B Transmit
SPIB_SIMO	6					I/O	SPI-B Slave Input, Master Output (SIMO)

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
SD1_D3	7					I	SDF-1 Channel 3 Data Input
SPIB_CLK	9					I/O	SPI-B Clock
GPIO21	0	—	—	—	—	I/O	General-Purpose Input/Output 21
QEP1_B	1					I	QEP-1 Input B
CANB_RX	3					I	CAN-B Receive
SPIB_SOMI	6					I/O	SPI-B Slave Output, Master Input (SOMI)
SD1_C3	7					I	SDF-1 Channel 3 Clock Input
I2CA_SCL	11					I/OD	I2C-A Open-Drain Bidirectional Clock
GPIO22	0, 4, 8, 12	83	67	56	51	I/O	General-Purpose Input/Output 22.
QEP1_STROBE	1					I/O	QEP-1 Gating
UARTB_TX	3					O	UART-B Transmit Data
SPIB_CLK	6					I/O	SPI-B Clock
SD1_D4	7					I	SDF-1 Channel 4 Data Input
LINA_TX	9					O	LIN-A Transmit
PWM4_A	5					O	PWM-4 Output A.
GPIO23	0	81	65	54	49	I/O	General-Purpose Input/Output 23.
QEP1_INDEX	1					I/O	QEP-1 index
UARTB_RX	3					I	UART-B Receive data
PWM4_B	5					O	PWM-4 Output B
SPIB_STE	6					I/O	SPI-B Slave Transmit Enable (STE)
SD1_C4	7					I	SDF-1 Channel 4 Clock Input

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
LINA_RX	9					I	LIN Receive
I2CA_SDA	11					O	I2C-A Open-Drain Bidirectional Data
SPIB_SIMO	13					I/O	SPI-B Slave Input, Master Output (SIMO)
GPIO24	0, 4, 8, 12	56	41	35	32	I/O	General-Purpose Input/Output 24
OUTPUTXBAR1	1					O	Output X-BAR Output 1
QEP2_A	2					I	QEP-2 Input A
PWM8_A	5					O	PWM-8 Output A
SPIB_SIMO	6					I/O	SPI-B Slave Input, Master Output (SIMO)
SD1_D1	7					I	SDF-1 Channel 1 Data Input
PMBUSA_SCL	10					I/OD	PMBus-A Open-Drain Bidirectional Clock
UARTA_TX	11					O	UART-A Transmit Data
ERRORSTS	13					O	Low-level valid error status output
TRACECLK	15					O	TRACE Clock
GPIO25	0, 4, 8, 12	57	42	—	—	I/O	General-Purpose Input/Output 25
OUTPUTXBAR2	1					O	Output X-BAR Output 2
QEP2_B	2					I	QEP-2 Input B
SPIB_SOMI	6					I/O	SPI-B Slave Output, Master Input (SOMI)
SD1_C1	7					I	SDF-1 Channel 1 Clock Input
PMBUSA_SDA	10					O	PMBus-A Open-Drain Bidirectional Data
UARTA_RX	11					I	UART-A Receive Data
QSPI_IO3	13					I/O	QSPI_IO3

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
QEP1_A	5					I	QEP-1 Input A
GPIO26	0, 4, 8, 12	58	43	—	—	I/O	General-Purpose Input/Output 26
OUTPUTXBAR3	1, 5					O	Output X-BAR Output 3
QEP2_INDEX	2					I/O	QEP-2 Index
SPIB_CLK	6					I/O	SPI-B Clock
SD1_D2	7					I	SDF-1 Channel 2 Data Input
PMBUSA_CTL	10					I	PMBus-A Control Signal
I2CA_SDA	11					I/OD	I2C-A Open-Drain Bidirectional Data
QSPI_IO2	13					I/O	QSPI_IO2
GPIO27	0, 4, 8, 12	59	44	—	—	I/O	General-Purpose Input/Output 27
OUTPUTXBAR4	1, 5					O	Output X-BAR Output 4
QEP2_STROBE	2					I/O	QEP-2 Gating
SPIB_STE	6					I/O	SPI-B Slave Transmit Enable (STE)
SD1_C2	7					I	SDF-1 Channel 2 Clock Input
PMBUSA_ALERT	10					I/OD	PMBus-A Open-Drain Bidirectional Alarm Signal
I2CA_SCL	11					I/OD	I2C-A Open-Drain Bidirectional Clock
QSPI_SCLK	13					I/O	QSPI_SCLK
GPIO28	0, 4, 8, 12	1	4	2	3	I/O	General-Purpose Input/Output 28
UARTA_RX	1					I	UART-A Receive Data
PWM7_A	3					O	PWM-7 Output A
OUTPUTXBAR5	5					O	Output X-BAR Output 5

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
QEP1_A	6					I	QEP-1 Input A
SD1_D3	7					I	SDF-1 Channel 3 Data Input
QEP2_STROBE	9					I/O	QEP-2 Gating
LINA_TX	10					O	LIN-A Transmit
SPIB_CLK	11					I/O	SPI-B Clock
ERRORSTS	13					O	Low-level valid error status output.
TRACECLK	15					I/O	TRACE Clock
GPIO29	0, 4, 8, 12					I/O	General-Purpose Input/Output 29
UARTA_TX	1					O	UART-A Transmit Data
PWM7_B	3					O	PWM-7 Output B
OUTPUTXBAR6	5					O	Output X-BAR Output 6
QEP1_B	6					I	QEP-1 Input B
SD1_C3	7	100	3	1	2	I	SDF-1 Channel 3 Clock Input
QEP2_INDEX	9					I/O	QEP-2 Index
LINA_RX	10					I	LIN-A Receive
SPIB_STE	11					I/O	SPI-B Slave Transmit Enable (STE)
ERRORSTS	13					O	Low-level valid error status output.
TRACED0	15					O	TRACE Synchronous Data Output 0
GPIO30	0, 4, 8, 12					I/O	General-Purpose Input/Output 30
CANA_RX	1	98	1	—	—	I	CAN-A Receive
SPIB_SIMO	3					I/O	SPI-B Slave Input, Master Output

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
OUTPUTXBAR7	5					O	Output X-BAR Output 7
QEP1_STROBE	6					I/O	QEP-1 Gating
SD1_D4	7					I	SDF-1 Channel 4 Data Input
QSPI_IO3	11					I/O	QSPI_IO3
PWM1_A	2					O	PWM 1 Output A
TRACED1	15					I/O	TRACE Synchronous Data Output 1
GPIO31	0, 4, 8, 12	99	2	—	—	I/O	General-Purpose Input/Output 31
CANA_TX	1					O	CAN-A Transmit
SPIB_SOMI	3					I/O	SPI-B Slave Output, Master Input (SOMI)
OUTPUTXBAR8	5					O	Output X-BAR Output 8
QEP1_INDEX	6					I/O	QEP-1 index
SD1_C4	7					I	SDF-1 Channel 4 Clock Input
QSPI_IO1	11					I/O	QSPI_IO1
PWM1_B	2					O	PWM 1 output B
TRACED2	15					I/O	TRACE Synchronous Data Output 2
GPIO32	0, 4, 8, 12	64	49	40	37	I/O	General-Purpose Input/Output 32
I2CA_SDA	1					I/OD	I2C-A Open-Drain Bidirectional Data
SPIB_CLK	3					I/O	SPI-B Clock
PWM8_B	5					O	PWM-8 Output B
LINA_TX	6					O	LIN-A Transmit
SD1_D3	7					I	SDF-1 Channel 3 Data Input

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
CANA_TX	10					O	CAN-A Transmit
QSPI_IO0	11					I/O	QSPI_IO0
ADCSOCBO	13					O	ADC conversion start B signal output to external ADC (from PWM)
TRGIO	15					I/O	External Trigger Bidirectional
GPIO33	0, 4, 8, 12	53	38	32	29	I/O	General-Purpose Input/Output 33
I2CA_SCL	1					I/OD	I2C-A Open-Drain Bidirectional Clock
SPIB_STE	3					I/O	SPI-B Slave Transmit Enable (STE)
OUTPUTXBAR4	5					O	Output X-BAR Output 4
LINA_RX	6					I	LIN-A Receive
SD1_C3	7					I	SDF-1 Channel 3 Clock Input
CANA_RX	10					I	CAN-A Receive
QSPI_SS_N	11					I/O	QSPI_SS_N
QEP2_B	2					I	QEP-2 Input B
ADCSOCAO	13					O	ADC conversion start A signal output to external ADC (from PWM)
TRACED1	15					I/O	TRACE Synchronous Data Output 1
GPIO34	0, 4, 8, 12	94	77	—	—	I/O	General-Purpose Input/Output 34
OUTPUTXBAR1	1					O	Output X-BAR Output 1
PMBUSA_SDA	6					I/OD	PMBus-A Open-Drain Bidirectional Data
GPIO35_TDI	0, 4, 8, 12	63	48	39	36	I/O	General-Purpose Input/Output 35
UARTA_RX	1					I	UART-A Receive Data

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
I2CA_SDA	3					I/OD	I2C-A Open-Drain Bidirectional Data
CANA_RX	5					I	CAN-A Receive
PMBUSA_SCL	6					I/OD	PMBus-A Open-Drain Bidirectional Clock
LINA_RX	7					I	LIN-A Receive
QEP1_A	9					I	QEP-1 Input A
PMBUSA_CTL	10					I	PMBus-A Control Signal
TDI	15					I	JTAG Test Data Input. Please refer to the "Pin Signal Description" for precautions.
GPIO37_TDO	0, 4, 8, 12	61	46	37	34	I/O	General-Purpose Input/Output 37
OUTPUTXBAR2	1					O	Output X-BAR Output 2
I2CA_SCL	3					I/OD	I2C-A Open-Drain Bidirectional Clock
UARTA_TX	5					O	UART-A Transmit Data
CANA_TX	6					O	CAN-A Transmit
LINA_TX	7					O	LIN-A Transmit
QEP1_B	9					I	QEP-1 Input B
PMBUSA_ALERT	10					I/OD	PMBus-A Open-Drain Bidirectional Alarm Signal
TDO	15					O	JTAG Test Data Output. Please refer to the "Pin Signal Description" for precautions.
GPIO39	0, 4, 8, 12	91	—	—	—	I/O	General-Purpose Input/Output 39
CANB_RX	6					I	CAN-B Receive
QSPI_IO3	11					I/O	QSPI_IO3
GPIO40	0, 4, 8, 12	85	—	—	—	I/O	General-Purpose Input/Output 40

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
PMBUSA_SDA	6					I/OD	PMBus-A Open-Drain Bidirectional Data
UARTB_TX	9					O	UART-B Transmit Data
QEP1_A	10					I	QEP-1 Input A
QSPI_IO2	11					I/O	QSPI_IO2
GPIO41	0, 4, 8, 12	—	66	—	—	I/O	General-Purpose Input/Output 41
PWM2_A	1					O	PWM 2 Output A
SPIB_STE	3					O	SPI-B Slave Transmit Enable
PMBUSA_SCL	6					I/OD	PMBus-A Open-Drain Bidirectional Clock
UARTB_RX	9					I	UART-B Receive data
QEP1_B	10					I	QEP-1 Input B
QSPI_SCLK	11					I/O	QSPI_SCLK
SPIB_SOMI	13					I/O	SPI-B Slave Output, Master Input
GPIO42	0, 4, 8, 12	—	57	—	—	I/O	General-Purpose Input/Output 42
LINA_RX	2					I	LIN-A Receive
OUTPUTXBAR5	3					O	Output X-BAR Output 5
PMBUSA_CTL	5					I	PMBus-A Control Signal
I2CA_SDA	6					I/OD	I2C-A Open-Drain Bidirectional Data
UARTB_TX	9					O	UART-B Transmit Data
QEP1_STROBE	10					O	QEP-1 Gating
GPIO43	0, 4, 8, 12	—	54	—	—	I/O	General-Purpose Input/Output 43
OUTPUTXBAR6	3					O	Output X-BAR Output 6

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
PMBUSA_ALERT	5					I/OD	PMBus-A Open-Drain Bidirectional Alarm Signal
I2CA_SCL	6					I/OD	I2C-A Open-Drain Bidirectional Clock
UARTB_RX	9					I	UART-B Receive data
QEP1_INDEX	10					I/O	QEP-1 index
GPIO44	0, 4, 8, 12	—	69	—	—	I/O	General-Purpose Input/Output 44
QEP1_A	2					I	QEP-1 Input A
OUTPUTXBAR7	3					O	Output X-BAR Output 7
QSPI_IO2	11					I/O	QSPI_IO2
GPIO45	0, 4, 8, 12	—	73	—	—	I/O	General-Purpose Input/Output 45
OUTPUTXBAR8	3					O	Output X-BAR Output 8
QSPI_IO0	11					I/O	QSPI_IO0
GPIO46	0, 4, 8, 12	—	6	—	—	I/O	General-Purpose Input/Output 46
LINA_TX	3					O	LIN-A Transmit
QSPI_SS_N	11					I/O	QSPI_SS_N
GPIO47	0, 4, 8, 12	—	64	—	—	I/O	General-Purpose Input/Output 47
PWM2_B	1					O	PWM-2 Output B
QEP1_A	2					I	QEP-1 Input A
LINA_RX	3					I	LIN-A Receive
SPIB_SIMO	6					I/O	SPI-B Slave Input, Master Output
PMBUSA_SDA	7					I/OD	PMBus-A Open-Drain Bidirectional Data
GPIO48	0, 4, 8, 12	—	—	—	—	I/O	General-Purpose Input/Output 48

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
OUTPUTXBAR3	1					O	Output X-BAR Output 3
CANB_TX	3					O	CAN-B Transmit Data
UARTA_TX	6					O	UART-A Transmit Data
SD1_D1	7					I	SDF-1 Channel 1 Data Input
GPIO49	0, 4, 8, 12	—	56	—	—	I/O	General-Purpose Input/Output 49
OUTPUTXBAR4	1					O	Output X-BAR Output 4
CANB_RX	3					I	CAN-B Receive
UARTA_RX	6					I	UART-A Receive Data
SD1_C1	7					I	SDF-1 Channel 1 Clock Input
QEP2_INDEX	9					I/O	QEP-2 Index
SYNCOUT	11					O	External PWM Synchronization Pulse
QEP1_INDEX	2					I/O	QEP-1 index
GPIO50	0, 4, 8, 12	—	—	—	—	I/O	General-Purpose Input/Output 50
QEP1_A	1					I	QEP-1 Input A
SPIB_SIMO	6					I/O	SPI-B Slave Input, Master Output (SIMO)
SD1_D2	7					I	SDF-1 Channel 2 Data Input
GPIO51	0, 4, 8, 12	—	—	—	—	I/O	General-Purpose Input/Output 51
QEP1_B	1					I	QEP-1 Input B
SPIB_SOMI	6					I/O	SPI-B Master Input, Slave Output (SOMI)
SD1_C2	7					I	SDF-1 Channel 2 Clock Input
GPIO52	0, 4, 8, 12	—	—	—	—	I/O	General-Purpose Input/Output 52

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
QEP1_STROBE	1					I/O	QEP-1 Input B Gating
SPIB_CLK	6					I/O	SPI-B Clock
SD1_D3	7					I	SDF-1 Channel 3 Data Input
GPIO53	0, 4, 8, 12	49	34	—	—	I/O	General-Purpose Input/Output 53
QEP1_INDEX	1					I/O	QEP-1 index
SPIB_STE	6					I/O	SPI-B Slave Transmit Enable (STE)
SD1_C3	7					I	SDF-1 Channel 3 Clock Input
UARTB_RX	9					I	UART-B Receive data
GPIO54	0, 4, 8, 12	48	33	—	—	I/O	General-Purpose Input/Output 54
SPIA_SIMO	1					I/O	SPI-A Slave Input, Master Output (SIMO)
QEP2_A	5					I	QEP-2 Input A
UARTB_TX	6					O	UART-B Transmit Data
SD1_D4	7					I	SDF-1 Channel 4 Data Input
GPIO55	0, 4, 8, 12	—	—	—	—	I/O	General-Purpose Input/Output 55
SPIA_SOMI	1					I/O	SPI-A Master Input, Slave Output (SOMI)
QEP2_B	5					I/O	QEP-2 Input B
UARTB_RX	6					I	UART-B Receive data
SD1_C4	7					I	SDF-1 Channel 4 Clock Input
GPIO56	0, 4, 8, 12	65	—	—	—	I/O	General-Purpose Input/Output 56
SPIA_CLK	1					I/O	SPI-A Clock
QEP2_STROBE	5					I/O	QEP-2 Gating

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
UARTB_TX	6					O	UART-B Transmit Data
SD1_D3	7					I	SDF-1 Channel 3 Data Input
SPIB_SIMO	9					I/O	SPI-B Slave Input, Master Output (SIMO)
QEP1_A	11					I	QEP-1 Input A
GPIO57	0, 4, 8, 12	66	—	—	—	I/O	General-Purpose Input/Output 57
SPIA_STE	1					I/O	SPI-A Slave Transmit Enable (STE)
QEP2_INDEX	5					I/O	QEP-2 Index
UARTB_RX	6					I	UART-B Receive data
SD1_C3	7					I	SDF-1 Channel 3 Clock Input
SPIB_SOMI	9					I/O	SPI-B Slave Output, Master Input (SOMI)
QEP1_B	11					I	QEP-1 Input B
GPIO58	0, 4, 8, 12	67	—	—	—	I/O	General-Purpose Input/Output 58
OUTPUTXBAR1	5					O	Output X-BAR Output 1
SPIB_CLK	6					I/O	SPI-B Clock
SD1_D4	7					I	SDF-1 Channel 4 Data Input
LINA_TX	9					O	LIN-A Transmit
CANB_TX	10					O	CAN-B Transmit
QEP1_STROBE	11					I/O	QEP-1 Gating
GPIO59	0, 4, 8, 12	92	—	—	—	I/O	General-Purpose Input/Output 59
OUTPUTXBAR2	5					O	Output X-BAR Output 2
SPIB_STE	6					I/O	SPI-B Slave Transmit Enable (STE)

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
SD1_C4	7					I	SDF-1 Channel 4 Clock Input
LINA_RX	9					I	LIN-A Receive
CANB_RX	10					I	CAN-B Receive
QEP1_INDEX	11					I/O	QEP-1 index
Debug and reset							
TCK（SWCLK）		60	45	36	33	I	JTAG test clock with an internal pull-up resistor. When used in SWD debugging mode, this pin can be used for SWD clock (SWCLK). Please refer to the "Pin Signal Description" for precautions.
TMS (SWDIO)		62	47	38	35	I/O	JTAG Test Mode Selection (TMS) with an internal pull-up resistor. When used in SWD debugging mode, this pin can be used for SWD serial data line (SWDIO). Please refer to the "Pin Signal Description" for precautions.
VREGENZ		73	—	46	—	I	Internal voltage regulator enable with an internal pull-down resistor. Please refer to the "Pin Signal Description" for precautions.
X1		69	51	42	39	I	Crystal oscillator or single-ended clock input. This pin can also be used to feed a single-ended 3.3V level clock. See "Pin Signal Description" section for precautions.
XRSn		2	5	3	4	I/OD	Device reset (input) and watchdog reset (output). The pin is active low. Please refer to the "Pin Signal Description" for precautions.
Power supply and grounding							
V_{DD}		4,46,71,87	8,31,53,71	4,27,44,59	5,24,41,53		1.1V digital logic power pin. Please refer to the "Pin

Signal name	Multiplexer location	LQFP100	LQFP80	LQFP64	QFN56	Pin type	Description
							Signal Description" for precautions.
V_{DDA}		11,34	26	22	20		3.3V analog power pin. Please refer to the "Pin Signal Description" for precautions.
VDDIO		3,47,70,80,88	7,32,72，52	28,43,53,60	25,40,48,54		3.3V digital I/O power pin. Please refer to the "Pin Signal Description" for precautions.
VSS		5,45,72,86	9,30,55,70	5, 26, 45, 58	—		Digital ground
VSSA		12,33	25	21	19		Analog ground
VSSIO		82		55	50		3.3V digital I/O ground

3.3. Pin Signal Description

3.3.1. Analog signal

Table 4 Analog Signals

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
A0	ADC-A Input 0	I		23	19	15	13
A1	ADC-A Input 1	I		22	18	14	12
A2	ADC-A Input 2	I		9	12	9	8
A3	ADC-A Input 3	I		10	13		
A4	ADC-A Input 4	I		36	27	23	21
A5	ADC-A Input 5	I		35			
A6	ADC-A Input 6	I		6	10	6	
A7	ADC-A Input 7	I		20			
A8	ADC-A Input 8	I		37			
A9	ADC-A Input 9	I		38	28		
A10	ADC-A Input 10	I		40	29	25	23
A11	ADC-A Input 11	I		18	16		
A12	ADC-A Input 12	I		30	22		
A14	ADC-A Input 14	I		16	15		
A15	ADC-A Input 15	I		14	14	10	9
AIO224	Digital Input 224 on ADC Pin	I		9	12	9	8
AIO225	Digital Input 225 on ADC Pin	I		36	27	23	21
AIO226	Digital Input 226 on ADC Pin	I		7	11	7	6
AIO227	Digital Input 227 on ADC Pin	I		39	28	24	22
AIO228	Digital Input 228 on ADC Pin	I		6	10	6	
AIO229	Digital Input 229 on ADC Pin	I		37			
AIO230	Digital Input 230 on ADC Pin	I		40	29	25	23
AIO231	Digital Input 231 on ADC Pin	I		23	19	15	13
AIO232	Digital Input 232 on ADC Pin	I		22	18	14	12
AIO233	Digital Input 233 on ADC Pin	I		10	13		
AIO234	Digital Input 234 on ADC Pin	I		35			
AIO235	Digital Input 235 on ADC Pin	I		20			
AIO236	Digital Input 236 on ADC Pin	I		38	28		

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
AIO237	Digital Input 237 on ADC Pin	I		19	16	12	10
AIO238	Digital Input 238 on ADC Pin	I		29	22	18	16
AIO239	Digital Input 239 on ADC Pin	I		17	15	11	
AIO240	Digital Input 240 on ADC Pin	I		28			
AIO241	Digital Input 241 on ADC Pin	I		41			
AIO242	Digital Input 242 on ADC Pin	I		8		8	7
AIO243	Digital Input 243 on ADC Pin	I		42			
AIO244	Digital Input 244 on ADC Pin	I		21	17	13	11
AIO245	Digital Input 245 on ADC Pin	I		31	23	19	17
AIO246	Digital Input 246 on ADC Pin	I		44			
AIO247	Digital Input 247 on ADC Pin	I		43			
AIO248	Digital Input 248 on ADC Pin	I		18	16		
AIO249	Digital Input 249 on ADC Pin	I		30	22		
AIO250	Digital Input 250 on ADC Pin	I		15	14	10	9
AIO251	Digital Input 251 on ADC Pin	I		13	13	10	9
AIO252	Digital Input 252 on ADC Pin	I		16	15		
AIO253	Digital Input 253 on ADC Pin	I		14	14	10	9
AIO254	Digital Input 254 on ADC Pin	I		32	24	20	18
B0	ADC-B Input 0	I		41			
B1	ADC-B Input 1	I		40	29	25	23
B2	ADC-B Input 2	I		7	11	7	6
B3	ADC-B Input 3	I		8		8	7
B4	ADC-B Input 4	I		39	28	24	22
B5	ADC-B Input 5	I		42			
B6	ADC-B Input 6	I		9	12	9	8
B7	ADC-B Input 7			18	16		
B8	ADC-B Input 8	I		36	27	23	21
B9	ADC-B Input 9	I		30	22		
B10	ADC-B Input 10	I		15	14	10	9
B11	ADC-B Input 11	I		13	13	10	9
B12	ADC-B Input 12	I		32	24	20	18
B15	ADC-B Input 15	I		23	19	15	13
C0	ADC-C Input 0	I		19	16	12	10

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
C1	ADC-C Input 1	I		29	22	18	16
C2	ADC-C Input 2	I		21	17	13	11
C3	ADC-C Input 3	I		31	23	19	17
C4	ADC-C Input 4	I		17	15	11	
C5	ADC-C Input 5	I		28			
C6	ADC-C Input 6	I		7	11	7	6
C7	ADC-C Input 7	I		15	14	10	9
C8	ADC-C Input 8	I		39	28	24	22
C9	ADC-C Input 9	I		13	13	10	9
C10	ADC-C Input 10	I		40	29	25	23
C11	ADC-C Input 11	I		32	24	20	18
C12	ADC-C Input 12	I		43			
C14	ADC-C Input 14	I		44			
C15	ADC-C Input 15	I		23	19	15	13
COMP1_HN0	COMP-1 High-level Comparator Negative Input 0	I		10	13		
COMP1_HN1	COMP-1 High-level Comparator Negative Input 1	I		19	16	12	10
COMP1_HP0	COMP-1 High-level Comparator Positive Input 0	I		9	12	9	8
COMP1_HP1	COMP-1 High-level Comparator Positive Input 1	I		19	16	12	10
COMP1_HP2	COMP-1 High-level Comparator Positive Input 2	I		18	16		
COMP1_HP3	COMP-1 High-level Comparator Positive Input 3	I		10	13		
COMP1_HP4	COMP-1 High-level Comparator Positive Input 4	I		18	16		
COMP1_LN0	COMP-1 Low-level Comparator Negative Input 0	I		10	13		
COMP1_LN1	COMP-1 Low-level Comparator Negative Input 1	I		19	16	12	10
COMP1_LP0	COMP-1 Low-level Comparator Positive Input 0	I		9	12	9	8
COMP1_LP1	COMP-1 Low-level Comparator Positive Input 1	I		19	16	12	10
COMP1_LP2	COMP-1 Low-level Comparator Positive Input 2	I		18	16		

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
COMP1_LP3	COMP-1 Low-level Comparator Positive Input 3	I		10	13		
COMP1_LP4	COMP-1 Low-level Comparator Positive Input 4	I		18	16		
COMP2_HN0	COMP-2 High-level Comparator Negative Input 0	I		35			
COMP2_HN1	COMP-2 High-level Comparator Negative Input 1	I		29	22	18	16
COMP2_HP0	COMP-2 High-level Comparator Positive Input 0	I		36	27	23	21
COMP2_HP1	COMP-2 High-level Comparator Positive Input 1	I		29	22	18	16
COMP2_HP2	COMP-2 High-level Comparator Positive Input 2	I		30	22		
COMP2_HP3	COMP-2 High-level Comparator Positive Input 3	I		35			
COMP2_HP4	COMP-2 High-level Comparator Positive Input 4	I		30	22		
COMP2_LN0	COMP-2 Low-level Comparator Negative Input 0	I		35			
COMP2_LN1	COMP-2 Low-level Comparator Negative Input 1	I		29	22	18	16
COMP2_LP0	COMP-2 Low-level Comparator Positive Input 0	I		36	27	23	21
COMP2_LP1	COMP-2 Low-level Comparator Positive Input 1	I		29	22	18	16
COMP2_LP2	COMP-2 Low-level Comparator Positive Input 2	I		30	22		
COMP2_LP3	COMP-2 Low-level Comparator Positive Input 3	I		35			
COMP2_LP4	COMP-2 Low-level Comparator Positive Input 4	I		30	22		
COMP3_HN0	COMP-3 High-level Comparator Negative Input 0	I		8		8	7
COMP3_HN1	COMP-3 High-level Comparator Negative Input 1	I		21	17	13	11
COMP3_HP0	COMP-3 High-level Comparator Positive Input 0	I		7	11	7	6
COMP3_HP1	COMP-3 High-level Comparator Positive Input 1	I		21	17	13	11
COMP3_HP2	COMP-3 High-level Comparator Positive Input 2	I		20			

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
COMP3_HP3	COMP-3 High-level Comparator Positive Input 3	I		8		8	7
COMP3_HP4	COMP-3 High-level Comparator Positive Input 4	I		15	14	10	9
COMP3_LN0	COMP-3 Low-level Comparator Negative Input 0	I		8		8	7
COMP3_LN1	COMP-3 Low-level Comparator Negative Input 1	I		21	17	13	11
COMP3_LP0	COMP-3 Low-level Comparator Positive Input 0	I		7	11	7	6
COMP3_LP1	COMP-3 Low-level Comparator Positive Input 1	I		21	17	13	11
COMP3_LP2	COMP-3 Low-level Comparator Positive Input 2	I		20			
COMP3_LP3	COMP-3 Low-level Comparator Positive Input 3	I		8		8	7
COMP3_LP4	COMP-3 Low-level Comparator Positive Input 4	I		15	14	10	9
COMP4_HN0	COMP-4 High-level Comparator Negative Input 0	I		42			
COMP4_HN1	COMP-4 High-level Comparator Negative Input 1	I		31	23	19	17
COMP4_HP0	COMP-4 High-level Comparator Positive Input 0	I		39	28	24	22
COMP4_HP1	COMP-4 High-level Comparator Positive Input 1	I		31	23	19	17
COMP4_HP2	COMP-4 High-level Comparator Positive Input 2	I		31	23	19	17
COMP4_HP3	COMP-4 High-level Comparator Positive Input 3	I		42			
COMP4_HP4	COMP-4 High-level Comparator Positive Input 4	I		13	13	10	9
COMP4_LN0	COMP-4 low-level comparator negative input 0	I		42			
COMP4_LN1	COMP-4 Low-level Comparator Negative Input 1	I		31	23	19	17
COMP4_LP0	COMP-4 Low-level Comparator Positive Input 0	I		39	28	24	22
COMP4_LP1	COMP-4 Low-level Comparator Positive Input 1	I		31	23	19	17
COMP4_LP2	COMP-4 Low-level Comparator Positive Input 2	I		31	23	19	17

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
COMP4_LP3	COMP-4 Low-level Comparator Positive Input 3	I		42			
COMP4_LP4	COMP-4 Low-level Comparator Positive Input 4	I		13	13	10	9
COMP5_HN0	COMP-5 High-level Comparator Negative Input 0	I		20			
COMP5_HN1	COMP-5 High-level Comparator Negative Input 1	I		17	15	11	
COMP5_HP0	COMP-5 High-level Comparator Positive Input 0	I		6	10	6	
COMP5_HP1	COMP-5 High-level Comparator Positive Input 1	I		17	15	11	
COMP5_HP2	COMP-5 High-level Comparator Positive Input 2	I		16	15		
COMP5_HP3	COMP-5 High-level Comparator Positive Input 3	I		20			
COMP5_HP4	COMP-5 High-level Comparator Positive Input 4	I		16	15		
COMP5_LN0	COMP-5 Low-level Comparator Negative Input 0	I		20			
COMP5_LN1	COMP-5 Low-level Comparator Negative Input 1	I		17	15	11	
COMP5_LP0	COMP-5 Low-level Comparator Positive Input 0	I		6	10	6	
COMP5_LP1	COMP-5 Low-level Comparator Positive Input1	I		17	15	11	
COMP5_LP2	COMP-5 Low-level Comparator Positive Input 2	I		16	15		
COMP5_LP3	COMP-5 Low-level Comparator Positive Input 3	I		20			
COMP5_LP4	COMP-5 Low-level Comparator Positive Input 4	I		16	15		
COMP6_HN0	COMP-6 High-level Comparator Negative Input 0	I		38	28		
COMP6_HN1	COMP-6 High-level Comparator Negative Input 1	I		28			
COMP6_HP0	COMP-6 High-level Comparator Positive Input 0	I		37			
COMP6_HP1	COMP-6 High-level Comparator Positive Input 1	I		28			
COMP6_HP2	COMP-6 High-level Comparator Positive Input 2	I		28			

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
COMP6_HP3	COMP-6 High-level Comparator Positive Input 3	I		38	28		
COMP6_HP4	COMP-6 High-level Comparator Positive Input 4	I		14	14	10	9
COMP6_LN0	COMP-6 Low-level Comparator Negative Input 0	I		38	28		
COMP6_LN1	COMP-6 Low-level Comparator Negative Input 1	I		28			
COMP6_LP0	COMP-6 Low-level Comparator Positive Input 0	I		37			
COMP6_LP1	COMP-6 Low-level Comparator Positive Input 1	I		28			
COMP6_LP2	COMP-6 Low-level Comparator Positive Input 2	I		28			
COMP6_LP3	COMP-6 Low-level Comparator Positive Input 3	I		38	28		
COMP6_LP4	COMP-6 Low-level Comparator Positive Input 4	I		14	14	10	9
COMP7_HN0	COMP-7 High-level Comparator Negative Input 0	I		41			
COMP7_HN1	COMP-7 High-level Comparator Negative Input 1	I		44			
COMP7_HP0	COMP-7 High-level Comparator Positive Input 0	I		40	29	25	23
COMP7_HP1	COMP-7 High-level Comparator Positive Input 1	I		44			
COMP7_HP2	COMP-7 High-level Comparator Positive Input 2	I		43			
COMP7_HP3	COMP-7 High-level Comparator Positive Input 3	I		41			
COMP7_HP4	COMP-7 High-level Comparator Positive Input 4	I		32	24	20	18
COMP7_LN0	COMP-7 Low-level Comparator Negative Input 0	I		41			
COMP7_LN1	COMP-7 Low-level Comparator Negative Input 1	I		44			
COMP7_LP0	COMP-7 Low-level Comparator Positive Input 0	I		40	29	25	23
COMP7_LP1	COMP-7 Low-level Comparator Positive Input 1	I		44			
COMP7_LP2	COMP-7 Low-level Comparator Positive Input 2	I		43			

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
COMP7_LP3	COMP-7 Low-level Comparator Positive Input 3	I		41			
COMP7_LP4	COMP-7 Low-level Comparator Positive Input 4	I		32	24	20	18
DACA_OUT	Buffer DAC-A Output	O		23	19	15	13
DACB_OUT	Buffer DAC-B Output	O		22	18	14	12
VDAC	Optional External Reference Voltage for On-chip DAC. If this pin is used as the reference for on-chip DAC, place at least one 1μF capacitor on this pin.	I		8		8	7
VREFHIA	ADC-A High Reference Voltage. Place at least one 2.2μF capacitor on this pin in internal or external reference mode. This capacitor should be placed as close to the device as possible between the VREFHIA and VREFLOA pins. Do not load this pin externally in internal or external reference mode.	I/O		25	20	16	14
VREFHIB	ADC-B High Reference Voltage. Place at least one 2.2μF capacitor on this pin in internal or external reference mode. This capacitor should be placed as close to the device as possible between the VREFHIB and VREFLOB pins. Do not load this pin externally in internal or external reference mode.	I/O		24	20	16	14
VREFHIC	ADC-C High Reference Voltage. Place at least one 2.2μF capacitor on this pin in internal or external reference mode. This capacitor should be placed as close to the device as possible between the VREFHIC and VREFLOC pins. Do not load this pin externally in internal or external reference mode.	I/O		24	20	16	14
VREFLOA	ADC-A Low Reference Voltage	I		27	21	17	15
VREFLOB	ADC-B Low Reference Voltage	I		26	21	17	15
VREFLOC	ADC-C Low Reference Voltage	I		26	21	17	15

3.3.2. Digital Signals

Table 5 Digital Signals

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
ADCSOCAO	ADC conversion start A signal output to external ADC (from PWM)	O	8, 33	74, 53	38, 58	47, 32	42, 29
ADCSOCBO	ADC conversion start B signal output to external ADC (from PWM)	O	10, 32	93, 64	76, 49	63, 40	37
CANA_RX	CAN-A Receive	I	18, 30, 33, 35, 5, 3, 12	68, 53, 63, 89, 98, 76, 51	50, 60, 74, 1, 36, 38, 48	41, 32, 39, 61, 49, 30	38, 29, 36, 55, 44, 27
CANA_TX	CAN-A Transmit	O	31,32, 37, 4, 13, 17, 2	61,64, 75, 99, 50, 55, 77	49, 59, 61, 2, 35, 40, 46	34, 37, 40, 48, 29, 50	34, 37, 43, 26, 31, 45
CANB_RX	CAN-B Receive	I	10, 13, 17, 39, 59, 7, 21, 49	50, 55, 84, 91, 92, 93, 51	56, 68, 76, 35, 40	29, 34, 57, 63	26, 31, 52
CANB_TX	CAN-B Transmit	O	12 16, 58, 6, 8, 20, 48	51, 54, 67, 74, 97	58, 80, 36, 39	30, 33, 47, 64	1, 27, 30, 42
PWM1_A	PWM-1 Output A	O	0, 30	79, 98	1, 63	52	47
PWM1_B	PWM-1 Output B	O	1, 31	78, 99	2, 62	51	46
PWM2_A	PWM-2 Output A	O	2, 41	77	61, 66	50	45
PWM2_B	PWM-2 Output B	O	3, 47	76	60, 64	49	44
PWM3_A	PWM-3 Output A	O	4, 14	75, 96	79, 59	48	43
PWM3_B	PWM-3 Output B	O	5, 15	89, 95	78, 74	61	55
PWM4_A	PWM-4 Output A	O	6, 22	97, 83	80, 67	64, 56	1, 51
PWM4_B	PWM-4 Output B	O	7, 23	84, 85	65, 68	57, 54	52, 49
PWM5_A	PWM-5 Output A	O	16, 8	54, 74	39, 58	33, 47	30, 42
PWM5_B	PWM-5 Output B	O	17, 9	55, 90	40, 75	34, 62	31, 56

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
PWM6_A	PWM-6 Output A	O	10, 18	68, 93	50, 76	41, 63	38
PWM6_B	PWM-6 Output B	O	11	52	37	31	28
PWM7_A	PWM-7 Output A	O	12, 28	1, 51	36, 4	2, 30	27, 3
PWM7_B	PWM-7 Output B	O	13, 29	100, 50	3, 35	1, 29	2, 26
PWM8_A	PWM-8 Output A	O	14, 24	56, 96	79, 41	35	32
PWM8_B	PWM-8 Output B	O	15, 32	64, 95	78, 49	40	37
QEP1_A	QEP-1 Input A	I	10, 28, 35, 40, 56, 6, 25, 47, 50, 20	1, 63, 65, 85, 93, 97, 57	4, 42, 48, 64, 69, 76, 80	2, 39, 63, 64	1, 3, 36
QEP1_B	QEP-1 Input B	I	11, 29, 37, 57, 7, 41, 51, 21	100, 52, 61, 66, 84	3, 37, 46, 66, 68	1, 31, 37, 57	2, 28, 34, 52
QEP1_INDEX	QEP-1 index	I/O	13, 17, 31, 59, 9, 53, 49, 43, 23	50, 55, 90, 92, 99, 49, 81	2, 35, 34, 40, 54, 56, 65, 75	29, 34, 62, 54	26, 31, 56, 49
QEP1_STROBE	QEP-1 Gating	I/O	12, 16, 22, 30, 58, 8, 52, 42	51, 54, 67, 74, 83, 98	1, 36, 39, 57, 58, 67	30, 33, 47, 56	27, 30, 42, 51
QEP2_A	QEP-2 Input A	I	14, 18, 24, 54, 11	56, 68, 96, 48, 52	37, 41, 50, 79, 33	35, 41, 31	32, 38, 28
QEP2_B	QEP-2 Input B	I	15, 25, 33, 16, 55	57, 95, 53, 54	38, 39, 42, 78	32, 33	29, 30
QEP2_INDEX	QEP-2 Index	I/O	26, 29, 57, 49	100, 58, 66	3, 43, 56	1	2
QEP2_STROBE	QEP-2 Gating	I/O	27, 28, 56, 4	1, 59, 65, 75	4, 44, 59	2, 48	3, 43
ERRORSTS	Low-level valid error status output. During power-on period or during failure period of the ERRORSTS signal itself, if an external pull-down resistor is used, the error state will be set to valid; if an external pull-up resistor is used, the error state will be set to invalid.	O	24, 28, 29	1, 100, 56	3, 4, 41	1, 2, 35	2, 3, 32

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
QSPI_SCLK	QSPI_SCLK		4, 27, 10, 41	75, 59, 93	66, 76, 44, 59	48, 63	43
QSPI_IO0	QSPI_IO0		12, 32, 6, 45	51, 64, 97	73, 80, 36, 49	30, 40, 64	27, 37, 1
QSPI_IO1	QSPI_IO1		11, 31, 0, 5	52, 99, 79, 89	74, 2, 37, 63	31, 52, 61	28, 47, 55
QSPI_IO2	QSPI_IO2		26, 3, 40, 9, 44	58, 76, 85, 90	75, 43, 60, 69	49, 62	44, 56
QSPI_IO3	QSPI_IO3		25, 8, 2, 39, 30	57, 74, 77, 91, 98	1, 42, 58, 61	47, 50	42, 45
QSPI_SS_N	QSPI_SS_N		13, 33, 7, 46	50, 53, 84	6, 35, 38, 68	29, 57, 32	26, 52, 29
GPIO0	General-Purpose Input/Output 0	I/O	0	79	63	52	47
GPIO1	General-Purpose Input/Output 1	I/O	1	78	62	51	46
GPIO2	General-Purpose Input/Output 2	I/O	2	77	61	50	45
GPIO3	General-Purpose Input/Output 3	I/O	3	76	60	49	44
GPIO4	General-Purpose Input/Output 4	I/O	4	75	59	48	43
GPIO5	General-Purpose Input/Output 5	I/O	5	89	74	61	55
GPIO6	General-Purpose Input/Output 6	I/O	6	97	80	64	1
GPIO7	General-Purpose Input/Output 7	I/O	7	84	68	57	52
GPIO8	General-Purpose Input/Output 8	I/O	8	74	58	47	42
GPIO9	General-Purpose Input/Output 9	I/O	9	90	75	62	56
GPIO10	General-Purpose Input/Output 10	I/O	10	93	76	63	
GPIO11	General-Purpose Input/Output 11	I/O	11	52	37	31	28
GPIO12	General-Purpose Input/Output 12	I/O	12	51	36	30	27
GPIO13	General-Purpose Input/Output 13	I/O	13	50	35	29	26
GPIO14	General-Purpose Input/Output 14	I/O	14	96	79		
GPIO15	General-Purpose Input/Output 15	I/O	15	95	78		
GPIO16	General-Purpose Input/Output 16	I/O	16	54	39	33	30
GPIO17	General-Purpose Input/Output 17	I/O	17	55	40	34	31
GPIO18_X2	General-Purpose Input/Output 18. Only when INTOSC is the system clock source and X1 is connected to an external pull-down	I/O	18	68	50	41	38

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
	resistor (1kΩ is recommended) , can this pin and its digital multiplexing option be used.						
GPIO20	General-Purpose Input/Output 20	I/O	20				
GPIO21	General-Purpose Input/Output 21	I/O	21				
GPIO22	General-Purpose Input/Output 22	I/O	22	83	67	56	51
GPIO23	General-Purpose Input/Output 23	I/O	23	81	65	54	49
GPIO24	General-Purpose Input/Output 24	I/O	24	56	41	35	32
GPIO25	General-Purpose Input/Output 25	I/O	25	57	42		
GPIO26	General-Purpose Input/Output 26	I/O	26	58	43		
GPIO27	General-Purpose Input/Output 27	I/O	27	59	44		
GPIO28	General-Purpose Input/Output 28	I/O	28	1	4	2	3
GPIO29	General-Purpose Input/Output 29	I/O	29	100	3	1	2
GPIO30	General-Purpose Input/Output 30	I/O	30	98	1		
GPIO31	General-Purpose Input/Output 31	I/O	31	99	2		
GPIO32	General-Purpose Input/Output 32	I/O	32	64	49	40	37
GPIO33	General-Purpose Input/Output 33	I/O	33	53	38	32	29
GPIO34	General-Purpose Input/Output 34	I/O	34	94	77		
GPIO35	General-Purpose Input/Output 35	I/O	35	63	48	39	36
GPIO37	General-Purpose Input/Output 37	I/O	37	61	46	37	34
GPIO39	General-Purpose Input/Output 39	I/O	39	91			
GPIO40	General-Purpose Input/Output 40	I/O	40	85			
GPIO41	General-Purpose Input/Output 41	I/O	41		66		
GPIO42	General-Purpose Input/Output 42	I/O	42		57		
GPIO43	General-Purpose Input/Output 43	I/O	43		54		
GPIO44	General-Purpose Input/Output 44	I/O	44		69		
GPIO45	General-Purpose Input/Output 45	I/O	45		73		
GPIO46	General-Purpose Input/Output 46	I/O	46		6		
GPIO47	General-Purpose Input/Output 47	I/O	47		64		
GPIO48	General-Purpose Input/Output 48	I/O	48				
GPIO49	General-Purpose Input/Output 49	I/O	49		56		
GPIO50	General-Purpose Input/Output 50	I/O	50				
GPIO51	General-Purpose Input/Output 51	I/O	51				

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
GPIO52	General-Purpose Input/Output 52	I/O	52				
GPIO53	General-Purpose Input/Output 53	I/O	53	49	34		
GPIO54	General-Purpose Input/Output 54	I/O	54	48	33		
GPIO55	General-Purpose Input/Output 55	I/O	55				
GPIO56	General-Purpose Input/Output 56	I/O	56	65			
GPIO57	General-Purpose Input/Output 57	I/O	57	66			
GPIO58	General-Purpose Input/Output 58	I/O	58	67			
GPIO59	General-Purpose Input/Output 59	I/O	59	92			
I2CA_SCL	I2C-A Open-Drain Bidirectional Clock	I/OD	1, 18, 27, 33, 37, 8, 21, 43	53, 59, 61, 68, 74, 78, 82	38, 44, 46, 50, 54, 58, 62	32, 37, 41, 47, 51, 55	29, 34, 38, 42, 46, 50
I2CA_SDA	I2C-A Open-Drain Bidirectional Data	I/OD	0, 10, 26, 32, 35, 23, 42	58, 63, 64, 79, 93, 81	43, 48, 49, 57, 63, 76, 65	39, 40, 52, 63, 54	36, 37, 47, 49
LINA_RX	LIN-A Receive	I	29, 33, 35, 59, 47, 47, 23	100, 53, 63, 92, 81	64, 57, 48, 38, 3, 65	1, 32, 39, 54	2, 29, 36, 49
LINA_TX	LIN-A Transmit	O	22, 28, 32, 37, 58, 46	1, 61, 64, 67, 83	4, 46 49, 6, 67	2, 37, 40, 56	3, 34, 37, 51
OUTPUTXBAR1	Output X-BAR Output 1	O	2, 24, 34, 58	56, 67, 77, 94	41, 61, 77	35, 50	32, 45
OUTPUTXBAR2	Output X-BAR Output 2	O	25, 3, 37, 59	57, 61, 76, 92	42, 46, 60	37, 49	34, 44
OUTPUTXBAR3	Output X-BAR Output 3	O	14, 26, 4, 5, 48	58, 75, 89, 96	43, 59, 74, 79	48, 61	43, 55
OUTPUTXBAR4	Output X-BAR Output 4	O	15, 27, 33, 6, 49	53, 59, 95, 97	38, 44, 78, 80, 56	32, 64	1, 29
OUTPUTXBAR5	Output X-BAR Output 5	O	28, 7, 42	1, 84	4, 57, 68	2, 57	3, 52
OUTPUTXBAR6	Output X-BAR Output 6	O	29, 9, 43	100, 90	3, 54, 75	1, 62	2, 56

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
OUTPUTXBAR7	Output X-BAR Output 7	O	11, 16, 30, 44	52, 54, 98	1, 37, 39, 69	31, 33	28, 30
OUTPUTXBAR8	Output X-BAR Output 8	O	17, 31, 45	55, 99	2, 40, 73	34	31
PMBUSA_ALERT	PMBus-A Open-Drain Bidirectional Alarm Signal	I/OD	13, 27, 37, 43	50, 59, 61	35, 44, 46, 54	29, 37	26, 34
PMBUSA_CTL	PMBus-A Control Signal	I	12, 18, 26, 35, 42	51, 58, 63, 68	36, 43, 48, 50, 57	30, 39，41	27, 36, 38
PMBUSA_SCL	PMBus-A Open-Drain Bidirectional Clock	I/OD	15, 16, 24, 3, 35, 41	54, 56, 63, 76, 95	39, 41, 48, 60, 66, 78	33, 35, 39, 49	30, 32, 36, 44
PMBUSA_SDA	PMBus-A Open-Drain Bidirectional Data	I/OD	14, 17, 2, 25, 34, 40, 47	55, 57, 77, 85, 94, 96	40, 42, 61, 64, 77, 79	34, 50	31, 45
UARTA_RX	UART-A Receive Data	I	17, 25, 28, 3, 35, 9, 49	1, 55, 57, 63, 76, 90	4, 40, 42, 48, 60, 75, 56	2, 34, 39, 49, 62	3, 31, 36, 44, 56
UARTA_TX	UART-A Transmit Data	O	16, 2, 24, 29, 37, 8, 48	100, 54, 56, 61, 74, 77	3, 39, 41, 46, 58, 61	1, 33, 35, 37, 47, 50	2, 30, 32, 34, 42, 45
UARTB_RX	UART-B Receive data	I	11, 13, 15, 57, 53, 55, 43, 41, 23	50, 52, 66, 95, 49, 81	65, 66, 78, 35, 37, 54, 34	29, 31, 54	26, 28, 49
UARTB_TX	UART-B Transmit Data	O	10, 12, 14, 18, 22, 40, 56, 9, 54, 42	51, 65, 68, 83, 85, 90, 93, 96, 48	67, 75, 76, 33, 57, 50, 79, 36	30, 41, 56, 62, 63	27, 38, 51, 56
SD1_C1	SDF-1 Channel 1 Clock Input	I	17, 25, 49	55, 57	40, 42, 56	34	31
SD1_C2	SDF-1 Channel 2 Clock Input	I	27, 51	59	44		
SD1_C3	SDF-1 Channel 3 Clock Input	I	29, 33, 57, 53,	100, 53, 66,	3, 34, 38	1, 32, 55	2, 29, 50

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
			21	49, 82			
SD1_C4	SDF-1 Channel 4 Clock Input	I	31, 59, 55, 23	92, 99, 81	65, 2, 38, 65	54	49
SD1_D1	SDF-1 Channel 1 Data Input	I	16, 24, 48	54, 56	39，41	33, 35	30, 32
SD1_D2	SDF-1 Channel 2 Data Input	I	18, 26, 50	58, 68	43, 50	41	38
SD1_D3	SDF-1 Channel 3 Data Input	I	28, 32, 56, 20, 52	1, 64, 65, 80	4, 49	2, 40, 53	3, 37, 48
SD1_D4	SDF-1 Channel 4 Data Input	I	22, 30, 58, 54	67, 83, 98, 48	33, 67, 1	56	51
SPIA_CLK	SPI-A Clock	I/O	18, 3, 56, 9, 12	65, 68, 76, 90, 51	36, 50, 60, 75	41, 49, 62, 30	38, 44, 56, 27
SPIA_SIMO	SPI-A Slave Input, Master Output	I/O	16, 8, 54, 11, 2	54, 74, 48, 52, 77, 33	37, 39, 58, 61	33, 47, 31, 50	30, 42, 28, 45
SPIA_SOMI	SPI-A Slave Output, Master Input	I/O	10, 17, 13, 1, 55	55, 93, 50, 78	35, 40, 62, 76	34, 63, 29, 51	31, 26, 46
SPIA_STE	SPI-A Slave Transmit Enable	I/O	11, 5, 57, 0	52, 66, 89, 79	37, 63, 74	31, 61, 52	28, 55, 47
SPIB_CLK	SPI-B Clock	I/O	14, 22, 26, 28, 32, 58, 4, 20, 52	1, 58, 64, 67, 83, 96, 75, 80	4, 43, 49, 59, 67, 79	2, 40, 56, 48, 53, 54	3, 37, 51, 43, 48, 49
SPIB_SIMO	SPI-B Slave Input, Master Output	I/O	24, 30, 56, 7, 20, 21, 23, 50	56, 65, 84, 98, 80, 81, 82	1, 41, 64, 68, 65	35, 57, 53, 55, 54	32, 52, 48, 50, 49
SPIB_SOMI	SPI-B Slave Output, Master Input	I/O	25, 31, 57, 6, 16, 21, 41, 51	57, 66, 97, 99, 54, 82	2, 39, 42, 66, 80	64, 33, 55	1, 30, 50
SPIB_STE	SPI-B Slave Transmit Enable	I/O	15, 27, 29, 33,	100, 53, 59,	3, 38, 44, 65,	1, 32	2, 29

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
			59, 53, 41, 23	92, 95, 49, 81	78		
SYNCOUT	External PWM Synchronization Pulse	O	6, 49	97	56, 80	64	1
X1	Crystal oscillator or single-ended clock input. This pin can also be used to feed in a single-ended 3.3V clock. The device initialization software must configure this pin before enabling the crystal oscillator. To use this oscillator, the quartz crystal circuit must be connected to X1 and X2. GPO19 is not supported. GPO19 is internally connected to the X1 function. When there is a need to use the X1 clock function, GPO19 should be maintained in input mode, and the pull-up resistor should be disabled to avoid interference with the X1 clock function.	I/O	-	69	51	42	39
X2	Crystal Oscillator Output	I/O	18	68	50	41	38
XCLKOUT	External Clock Output	O	16, 18	54, 68	39, 50	33, 41	30, 38

3.3.3. Power supply and grounding

Table 6 Power Supply and Grounding

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
V_{DD}	1.1V digital logic power pin. It is recommended to place a decoupling capacitor with a minimum total capacitance of approximately 20μF near each VDD pin.			4, 46, 71, 87	31, 53, 71, 8	27, 4, 44, 59	24, 41, 5, 53
V_{DDA}	3.3V analog power pin. It is recommended to place a decoupling capacitor on each pin with a minimum value of 2.2μF and connected to VSSA.			11, 34	26	22	20
VDDIO	3.3V digital I/O power pin. It is recommended to place on each pin a decoupling capacitor with a minimum value of 0.1μF.			3, 47, 70, 80, 88	32, 52, 7, 72	28, 43, 53, 60	25, 40, 48, 54
VSS	Digital ground			45, 5, 72, 86	30, 55, 70, 9	26, 45, 5, 58	
VSSA	Analog ground			12, 33	25	21	19
VSSIO	3.3V digital I/O ground			82		55	50

3.3.4. Debug and reset

Table 7 Test and Reset

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
TCK（SWCLK）	JTAG test clock with an internal pull-up resistor. When used in SWD debugging mode, this pin can be used for SWD clock (SWCLK).	I		60	45	36	33
TMS (SWDIO)	JTAG test mode selection with an internal pull-up resistor；when SWD debug mode is used, this pin can be used for SWD serial data line (SWDIO).	I/O		62	47	38	35
TDI	JTAG test data input (TDI). By default, the internal pull-up resistor is disabled. If this pin is used as JTAG TDI, the internal pull-up resistor should be enabled or an external pull-up resistor should be added to avoid input suspension.	I	35	63	48	39	36
TDO	JTAG test data output (TDO). By default, the internal pull-up resistor is disabled. When there is no JTAG activity, the TDO function will be under a three-state condition, causing this pin to be suspended; the internal pull-up resistors should be enabled or an external pull-up resistor should be added to avoid GPIO input suspension.	O	37	61	46	37	34
VREGENZ	Internal voltage regulator enable with an internal pull-down resistor. Directly connect to VSS (low level) to enable internal VREG, or directly connect to VDDIO (high level) to use the external power supply.	I		73		46	

Signal name	Description	Pin type	GPIO	LQFP100	LQFP80	LQFP64	QFN56
XRSn	Device reset (input) and watchdog reset (output). When powered on, this pin is driven to a low level by the device, and the external circuit may also drive this pin to make the chip reset take effect; when a watchdog reset occurs, this pin is also driven to a low level by the MCU. A pull-up resistor with a resistance between 2.2kΩ and 10kΩ should be placed between XRSn and VDDIO, and it is recommended to place a pull-down capacitor with a resistance of less than 100nF between XRSn and VSS for noise filtering. When the watchdog reset takes effect, these values enable the watchdog to correctly drive the XRSn pin to VOL within 512 OSCCLK cycles. The output buffer of this pin is an open-drain device with an internal pull-up resistor. When this pin is driven by an external device, an open-drain device should be used for driving.	I/OD		2	5	3	4

3.4. Multiplexing of Pins

3.4.1. GPIO Multiplexing Pins

The table below lists the GPIO multiplexing pins. The default mode for each GPIO pin is GPIO function, except for GPO35 and GPO37. The default mode of these two pins is TDI and TDO respectively. The auxiliary functions can be selected by setting GPyGMUXn.GPIOz and GPyMUXn.GPIOz registers. The GPyGMUXn register should be configured before GPyMUXn to prevent alternating multiplexer selection from causing transient pulses to GPIO. The columns not displayed and the blank cells are reserved GPIO multiplexer settings.

Note: GPIO20, GPIO21, GPIO48, GPIO50, GPIO51, GPIO52, and GPIO55 are not available on any package. The boot ROM enables the pull-up resistors on these pins.

Table 8 GPIO Multiplexing Pins

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15
GPIO0	PWM1_A		SPIA_STE		I2CA_SDA				QSPI_IO1			
GPIO1	PWM1_B		SPIA_SOMI		I2CA_SCL							
GPIO2	PWM2_A	CANA_TX	SPIA_SIMO	OUTPUTXBAR1	PMBUSA_SDA		UARTA_TX		QSPI_IO3			
GPIO3	PWM2_B	OUTPUTXBAR2	CANA_RX	OUTPUTXBAR2	PMBUSA_SCL	SPIA_CLK	UARTA_RX		QSPI_IO2			
GPIO4	PWM3_A	QEP2_STROBE	SPIB_CLK	OUTPUTXBAR3	CANA_TX				QSPI_SCLK			
GPIO5	PWM3_B		OUTPUTXBAR3		CANA_RX	SPIA_STE			QSPI_IO1			
GPIO6	PWM4_A	OUTPUTXBAR4	SYNCOUT	QEP1_A	CANB_TX	SPIB_SOMI			QSPI_IO0			
GPIO7	PWM4_B		OUTPUTX	QEP1_B	CANB_RX	SPIB_SIMO			QSPI_SS_			

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15
			BAR5						N			
GPIO8	PWM5_A	CANB_TX	ADCSOCAO	QEP1_STROBE	UARTA_TX	SPIA_SIMO	I2CA_SCL		QSPI_IO3			
GPIO9	PWM5_B	UARTB_TX	OUTPUTXBAR6	QEP1_INDEX	UARTA_RX	SPIA_CLK			QSPI_IO2			
GPIO10	PWM6_A	CANB_RX	ADCSOCBO	QEP1_A	UARTB_TX	SPIA_SOMI	I2CA_SDA		QSPI_SCLK			
GPIO11	PWM6_B	UARTB_RX	OUTPUTXBAR7	QEP1_B	UARTB_RX	SPIA_STE		QEP2_A	QSPI_IO1	SPIA_SIMO		
GPIO12	PWM7_A	CANB_TX	SPIA_CLK	QEP1_STROBE	UARTB_TX	PMBUSA_CTL		CANA_RX	QSPI_IO0			TRACED2
GPIO13	PWM7_B	CANB_RX	SPIA_SOMI	QEP1_INDEX	UARTB_RX	PMBUSA_ALERT		CANA_TX	QSPI_SS_N			TRACED3
GPIO14	PWM8_A	UARTB_TX		PWM3_A	OUTPUTXBAR3	PMBUSA_SDA	SPIB_CLK	QEP2_A				
GPIO15	PWM8_B	UARTB_RX		PWM3_B	OUTPUTXBAR4	PMBUSA_SCL	SPIB_STE	QEP2_B				
GPIO16	SPIA_SIMO	CANB_TX	OUTPUTXBAR7	PWM5_A	UARTA_TX	SD1_D1	QEP1_STROBE	PMBUSA_SCL	XCLKOUT	SPIB_SOMI	QEP2_B	TRACED0
GPIO17	SPIA_SOMI	CANB_RX	OUTPUTXBAR8	PWM5_B	UARTA_RX	SD1_C1	QEP1_INDEX	PMBUSA_SDA		CANA_TX		TRGIO
GPIO18_X2	SPIA_CLK	UARTB_TX	CANA_RX	PWM6_A	I2CA_SCL	SD1_D2	QEP2_A	PMBUSA_CTL	XCLKOUT			
GPIO20	QEP1_A		CANB_TX		SPIB_SIMO	SD1_D3	SPIB_CLK					
GPIO21	QEP1_B		CANB_RX		SPIB_SOM	SD1_C3			I2CA_SCL			

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15
					I							
GPIO22	QEP1_STROBE		UARTB_TX	PWM4_A	SPIB_CLK	SD1_D4	LINA_TX					
GPIO23	QEP1_INDEX		UARTB_RX	PWM4_B	SPIB_STE	SD1_C4	LINA_RX		I2CA_SDA	SPIB_SIMO		
GPIO24	OUTPUTXBAR1	QEP2_A		PWM8_A	SPIB_SIMO	SD1_D1		PMBUSA_SCL	UARTA_TX	ERRORSTS		TRACECLK
GPIO25	OUTPUTXBAR2	QEP2_B		QEP1_A	SPIB_SOMI	SD1_C1		PMBUSA_SDA	UARTA_RX	QSPI_IO3		
GPIO26	OUTPUTXBAR3	QEP2_INDEX		OUTPUTXBAR3	SPIB_CLK	SD1_D2		PMBUSA_CTL	I2CA_SDA	QSPI_IO2		
GPIO27	OUTPUTXBAR4	QEP2_STROBE		OUTPUTXBAR4	SPIB_STE	SD1_C2		PMBUSA_ALERT	I2CA_SCL	QSPI_SCLK		
GPIO28	UARTA_RX		PWM7_A	OUTPUTXBAR5	QEP1_A	SD1_D3	QEP2_STROBE	LINA_TX	SPIB_CLK	ERRORSTS		TRACECLK
GPIO29	UARTA_TX		PWM7_B	OUTPUTXBAR6	QEP1_B	SD1_C3	QEP2_INDEX	LINA_RX	SPIB_STE	ERRORSTS		TRACED0
GPIO30	CANA_RX	PWM1_A	SPIB_SIMO	OUTPUTXBAR7	QEP1_STROBE	SD1_D4			QSPI_IO3			TRACED1
GPIO31	CANA_TX	PWM1_B	SPIB_SOMI	OUTPUTXBAR8	QEP1_INDEX	SD1_C4			QSPI_IO1			TRACED2
GPIO32	I2CA_SDA		SPIB_CLK	PWM8_B	LINA_TX	SD1_D3		CANA_TX	QSPI_IO0	ADCSOCBO		TRGIO
GPIO33	I2CA_SCL	QEP2_B	SPIB_STE	OUTPUTXBAR4	LINA_RX	SD1_C3		CANA_RX	QSPI_SS_N	ADCSOCAO		TRACED1
GPIO34	OUTPUTXBAR1				PMBUSA_SDA							TRACED3

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15
GPIO35	UARTA_RX		I2CA_SDA	CANA_RX	PMBUSA_SCL	LINA_RX	QEP1_A	PMBUSA_CTL				TDI
GPIO37	OUTPUTXBAR2		I2CA_SCL	UARTA_TX	CANA_TX	LINA_TX	QEP1_B	PMBUSA_ALERT				TDO
GPIO39					CANB_RX				QSPI_IO3			
GPIO40					PMBUSA_SDA		UARTB_TX	QEP1_A	QSPI_IO2			
GPIO41	PWM2_A		SPIB_STE		PMBUSA_SCL		UARTB_RX	QEP1_B	QSPI_SCLK	SPIB_SOMI		
GPIO42		LINA_RX	OUTPUTXBAR5	PMBUSA_CTL	I2CA_SDA		UARTB_RX	QEP1_STROBE				
GPIO43			OUTPUTXBAR6	PMBUSA_ALERT	I2CA_SCL		UARTB_TX	QEP1_INDEX				
GPIO44		QEP1_A	OUTPUTXBAR7						QSPI_IO2			
GPIO45			OUTPUTXBAR8						QSPI_IO0			
GPIO46			LINA_TX						QSPI_SS_N			
GPIO47	PWM2_B	QEP1_A	LINA_RX		SPIB_SIMO	PMBUSA_SDA						
GPIO48	OUTPUTXBAR3		CANB_TX		UARTA_TX	SD1_D1						
GPIO49	OUTPUTXBAR4	QEP1_INDEX	CANB_RX		UARTA_RX	SD1_C1	QEP2_INDEX		SYNCOUT			
GPIO50	QEP1_A				SPIB_SIM	SD1_D2						

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15
					O							
GPIO51	QEP1_B				SPIB_SOMI	SD1_C2						
GPIO52	QEP1_STROBE				SPIB_CLK	SD1_D3						
GPIO53	QEP1_INDEX				SPIB_STE	SD1_C3	UARTB_RX					
GPIO54	SPIA_SIMO			QEP2_A	UARTB_TX	SD1_D4						
GPIO55	SPIA_SOMI			QEP2_B	UARTB_RX	SD1_C4						
GPIO56	SPIA_CLK			QEP2_STROBE	UARTB_TX	SD1_D3	SPIB_SIMO		QEP1_A			
GPIO57	SPIA_STE			QEP2_INDEX	UARTB_RX	SD1_C3	SPIB_SOMI		QEP1_B			
GPIO58				OUTPUTXBAR1	SPIB_CLK	SD1_D4	LINA_TX	CANB_TX	QEP1_STROBE			
GPIO59				OUTPUTXBAR2	SPIB_STE	SD1_C4	LINA_RX	CANB_RX	QEP1_INDEX			

The digital signal and corresponding GPIO table lists all available multiplexed signals in each package and corresponding GPIO.

Table 9 Digital Signals and Corresponding GPIO

Signal name	Pin type	Description	LQFP100	LQFP80	LQFP64	QFN56
ADCSOCAO	O	ADC conversion from an external ADC (from PWM module) starts A output	GPIO8 GPIO33	GPIO8 GPIO33	GPIO8 GPIO33	GPIO8 GPIO33
ADCSOCBO	O	ADC conversion from an external	GPIO10	GPIO10	GPIO10	GPIO32

Signal name	Pin type	Description	LQFP100	LQFP80	LQFP64	QFN56
		ADC (from PWM module) starts B output	GPIO32	GPIO32	GPIO32	
CANA_RX	I	CAN-A Receive	GPIO3 GPIO5 GPIO12 GPIO18_X2 GPIO30 GPIO33 GPIO35/TDI	GPIO3 GPIO5 GPIO12 GPIO18_X2 GPIO30 GPIO33 GPIO35/TDI	GPIO3 GPIO5 GPIO12 GPIO18_X2 GPIO33 GPIO35/TDI	GPIO3 GPIO5 GPIO12 GPIO18_X2 GPIO33 GPIO35/TDI
CANA_TX	O	CAN-A Transmit	GPIO2 GPIO4 GPIO13 GPIO17 GPIO31 GPIO32 GPIO37/TDO	GPIO2 GPIO4 GPIO13 GPIO17 GPIO31 GPIO32 GPIO37/TDO	GPIO2 GPIO4 GPIO13 GPIO17 GPIO32 GPIO37/TDO	GPIO2 GPIO4 GPIO13 GPIO17 GPIO32 GPIO37/TDO
CANB_RX	I	CAN-B Receive	GPIO7 GPIO10 GPIO13 GPIO17 GPIO21 GPIO39 GPIO59	GPIO7 GPIO10 GPIO13 GPIO17 GPIO49	GPIO7 GPIO10 GPIO13 GPIO17 GPIO21	GPIO7 GPIO13 GPIO17 GPIO21
CANB_TX	O	CAN-B Transmit	GPIO6 GPIO8 GPIO12 GPIO16 GPIO20	GPIO6 GPIO8 GPIO12 GPIO16	GPIO6 GPIO8 GPIO12 GPIO16 GPIO20	GPIO6 GPIO8 GPIO12 GPIO16 GPIO20

Signal name	Pin type	Description	LQFP100	LQFP80	LQFP64	QFN56
			GPIO58			
PWM1_A	O	PWM-1 Output A	GPIO0 GPIO30	GPIO0 GPIO30	GPIO0	GPIO0
PWM1_B	O	PWM-1 Output B	GPIO1 GPIO31	GPIO1 GPIO31	GPIO1	GPIO1
PWM2_A	O	PWM-2 Output A	GPIO2	GPIO2 GPIO41	GPIO2	GPIO2
PWM2_B	O	PWM-2 Output B	GPIO3	GPIO3 GPIO47	GPIO3	GPIO3
PWM3_A	O	PWM-3 Output A	GPIO4 GPIO14	GPIO4 GPIO14	GPIO4	GPIO4
PWM3_B	O	PWM-3 Output B	GPIO5 GPIO15	GPIO5 GPIO15	GPIO5	GPIO5
PWM4_A	O	PWM-4 Output A	GPIO6 GPIO22	GPIO6 GPIO22	GPIO6 GPIO22	GPIO6 GPIO22
PWM4_B	O	PWM-4 Output B	GPIO7 GPIO23	GPIO7 GPIO23	GPIO7 GPIO23	GPIO7 GPIO23
PWM5_A	O	PWM-5 Output A	GPIO8 GPIO16	GPIO8 GPIO16	GPIO8 GPIO16	GPIO8 GPIO16
PWM5_B	O	PWM-5 Output B	GPIO9 GPIO17	GPIO9 GPIO17	GPIO9 GPIO17	GPIO9 GPIO17
PWM6_A	O	PWM-6 Output A	GPIO10 GPIO18_X2	GPIO10 GPIO18_X2	GPIO10 GPIO18_X2	GPIO18_X2
PWM6_B	O	PWM-6 Output B	GPIO11	GPIO11	GPIO11	GPIO11
PWM7_A	O	PWM-7 Output A	GPIO12 GPIO28	GPIO12 GPIO28	GPIO12 GPIO28	GPIO12 GPIO28
PWM7_B	O	PWM-7 Output B	GPIO13	GPIO13	GPIO13	GPIO13

Signal name	Pin type	Description	LQFP100	LQFP80	LQFP64	QFN56
			GPIO29	GPIO29	GPIO29	GPIO29
PWM8_A	O	PWM-8 Output A	GPIO14 GPIO24	GPIO14 GPIO24	GPIO24	GPIO24
PWM8_B	O	PWM-8 Output B	GPIO15 GPIO32	GPIO15 GPIO32	GPIO32	GPIO32
QEP1_A	I	QEP-1 Input A	GPIO6 GPIO10 GPIO25 GPIO28 GPIO35/TDI GPIO40 GPIO56	GPIO6 GPIO10 GPIO44 GPIO25 GPIO28 GPIO35/TDI GPIO47	GPIO6 GPIO10 GPIO28 GPIO35/TDI	GPIO6 GPIO28 GPIO35/TDI
QEP1_B	I	QEP-1 Input B	GPIO7 GPIO11 GPIO29 GPIO37/TDO GPIO57	GPIO7 GPIO11 GPIO29 GPIO37/TDO GPIO41	GPIO7 GPIO11 GPIO29 GPIO37/TDO	GPIO7 GPIO11 GPIO29 GPIO37/TDO
QEP1_INDEX	I/O	QEP-1 index	GPIO9 GPIO13 GPIO17 GPIO23 GPIO31 GPIO53 GPIO59	GPIO9 GPIO13 GPIO17 GPIO23 GPIO31 GPIO43 GPIO49 GPIO53	GPIO9 GPIO13 GPIO17 GPIO23	GPIO9 GPIO13 GPIO17 GPIO23
QEP1_STROBE	I/O	QEP-1 Gating	GPIO8 GPIO12 GPIO16	GPIO8 GPIO12 GPIO16	GPIO8 GPIO12 GPIO16	GPIO8 GPIO12 GPIO16

Signal name	Pin type	Description	LQFP100	LQFP80	LQFP64	QFN56
			GPIO22 GPIO30 GPIO58	GPIO22 GPIO30 GPIO42	GPIO22	GPIO22
QEP2_A	I	QEP-2 Input A	GPIO11 GPIO14 GPIO18_X2 GPIO24 GPIO54	GPIO11 GPIO14 GPIO18_X2 GPIO24 GPIO54	GPIO11 GPIO18_X2 GPIO24	GPIO11 GPIO18_X2 GPIO24
QEP2_B	I	QEP-2 Input B	GPIO15 GPIO16 GPIO25 GPIO33	GPIO15 GPIO16 GPIO25 GPIO33	GPIO16 GPIO33	GPIO16 GPIO33
QEP2_INDEX	I/O	QEP-2 Index	GPIO26 GPIO29 GPIO57	GPIO26 GPIO29 GPIO49	GPIO29	GPIO29
QEP2_STROBE	I/O	QEP-2 Gating	GPIO4 GPIO27 GPIO28 GPIO56	GPIO4 GPIO27 GPIO28	GPIO4 GPIO28	GPIO4 GPIO28
ERRORSTS	O	Low-level valid error status output. If you want to set the error state to valid during power on or when the ERRORSTS signal fails, an external pull-down resistor can be used. If you do not want to set the error state to valid under the above conditions, a pull-up resistor can be used.	GPIO24 GPIO28 GPIO29	GPIO24 GPIO28 GPIO29	GPIO24 GPIO28 GPIO29	GPIO24 GPIO28 GPIO29
QSPI_IO0	IO	QSPI Data Input/Output 0	GPIO6	GPIO6	GPIO6	GPIO6

Signal name	Pin type	Description	LQFP100	LQFP80	LQFP64	QFN56
			GPIO12 GPIO32	GPIO12 GPIO32 GPIO45	GPIO12 GPIO32	GPIO12 GPIO32
QSPI_IO1	IO	QSPI Data Input/Output 1	GPIO0 GPIO5 GPIO11 GPIO31	GPIO0 GPIO5 GPIO11 GPIO31	GPIO0 GPIO5 GPIO11	GPIO0 GPIO5 GPIO11
QSPI_IO2	IO	QSPI Data Input/Output 2	GPIO3 GPIO9 GPIO26 GPIO40	GPIO3 GPIO9 GPIO26 GPIO44	GPIO3 GPIO9	GPIO3 GPIO9
QSPI_IO3	IO	QSPI Data Input/Output 3	GPIO2 GPIO8 GPIO25 GPIO30 GPIO39	GPIO2 GPIO8 GPIO25 GPIO30	GPIO2 GPIO8	GPIO2 GPIO8
QSPI_SCLK	O	QSPI Clock Output	GPIO4 GPIO10 GPIO27	GPIO4 GPIO10 GPIO27 GPIO41	GPIO4 GPIO10	GPIO4
QSPI_SS_N	O	QSPI Chip Selection Output	GPIO7 GPIO13 GPIO33	GPIO7 GPIO13 GPIO46 GPIO33	GPIO7 GPIO13 GPIO33	GPIO7 GPIO13 GPIO33
I2CA_SCL	I/OD	I2C-A Open-Drain Bidirectional Clock	GPIO1 GPIO8 GPIO18_X2 GPIO27	GPIO1 GPIO8 GPIO18_X2 GPIO27	GPIO1 GPIO8 GPIO18_X2 GPIO33	GPIO1 GPIO8 GPIO18_X2 GPIO33

Signal name	Pin type	Description	LQFP100	LQFP80	LQFP64	QFN56
			GPIO33 GPIO37/TDO	GPIO33 GPIO37/TDO GPIO43	GPIO37/TDO	GPIO37/TDO
I2CA_SDA	I/OD	I2C-A Open-Drain Bidirectional Data	GPIO0 GPIO10 GPIO23 GPIO26 GPIO32 GPIO35/TDI	GPIO0 GPIO10 GPIO23 GPIO26 GPIO32 GPIO35/TDI GPIO42	GPIO0 GPIO10 GPIO23 GPIO32 GPIO35/TDI	GPIO0 GPIO23 GPIO32 GPIO35/TDI
LINA_RX	I	LIN-A Receive	GPIO23 GPIO29 GPIO33 GPIO35/TDI GPIO59	GPIO23 GPIO29 GPIO33 GPIO35/TDI GPIO42 GPIO47	GPIO23 GPIO29 GPIO33 GPIO35/TDI	GPIO23 GPIO29 GPIO33 GPIO35/TDI
LINA_TX	O	LIN-A Transmit	GPIO22 GPIO28 GPIO32 GPIO37/TDO GPIO58	GPIO22 GPIO28 GPIO32 GPIO37/TDO GPIO46	GPIO22 GPIO28 GPIO32 GPIO37/TDO	GPIO22 GPIO28 GPIO32 GPIO37/TDO
OUTPUTXBAR1	O	Output X-BAR Output 1	GPIO2 GPIO24 GPIO34 GPIO58	GPIO2 GPIO24 GPIO34	GPIO2 GPIO24	GPIO2 GPIO24
OUTPUTXBAR2	O	Output X-BAR Output 2	GPIO3 GPIO25 GPIO37/TDO	GPIO3 GPIO25 GPIO37/TDO	GPIO3 GPIO37/TDO	GPIO3 GPIO37/TDO

Signal name	Pin type	Description	LQFP100	LQFP80	LQFP64	QFN56
			GPIO59			
OUTPUTXBAR3	O	Output X-BAR Output 3	GPIO4 GPIO5 GPIO14 GPIO26	GPIO4 GPIO5 GPIO14 GPIO26	GPIO4 GPIO5	GPIO4 GPIO5
OUTPUTXBAR4	O	Output X-BAR Output 4	GPIO6 GPIO15 GPIO27 GPIO33	GPIO6 GPIO15 GPIO27 GPIO33 GPIO49	GPIO6 GPIO33	GPIO6 GPIO33
OUTPUTXBAR5	O	Output X-BAR Output 5	GPIO7 GPIO28	GPIO7 GPIO28 GPIO42	GPIO7 GPIO28	GPIO7 GPIO28
OUTPUTXBAR6	O	Output X-BAR Output 6	GPIO9 GPIO29	GPIO9 GPIO29 GPIO43	GPIO9 GPIO29	GPIO9 GPIO29
OUTPUTXBAR7	O	Output X-BAR Output 7	GPIO11 GPIO16 GPIO30	GPIO11 GPIO16 GPIO30 GPIO44	GPIO11 GPIO16	GPIO11 GPIO16
OUTPUTXBAR8	O	Output X-BAR Output 8	GPIO17 GPIO31	GPIO17 GPIO31 GPIO45	GPIO17	GPIO17
PMBUSA_ALERT	I/OD	PMBus-A Open-Drain Bidirectional Alarm Signal	GPIO13 GPIO27 GPIO37/TDO	GPIO13 GPIO27 GPIO37/TDO GPIO43	GPIO13 GPIO37/TDO	GPIO13 GPIO37/TDO

Signal name	Pin type	Description	LQFP100	LQFP80	LQFP64	QFN56
PMBUSA_CTL	I	PMBus-A Control Signal	GPIO12 GPIO18_X2 GPIO26 GPIO35/TDI	GPIO12 GPIO18_X2 GPIO26 GPIO35/TDI GPIO42	GPIO12 GPIO18_X2 GPIO35/TDI	GPIO12 GPIO18_X2 GPIO35/TDI
PMBUSA_SCL	I/OD	PMBus-A Open-Drain Bidirectional Clock	GPIO3 GPIO15 GPIO16 GPIO24 GPIO35/TDI	GPIO3 GPIO15 GPIO16 GPIO24 GPIO35/TDI GPIO41	GPIO3 GPIO16 GPIO24 GPIO35/TDI	GPIO3 GPIO16 GPIO24 GPIO35/TDI
PMBUSA_SDA	I/OD	PMBus-A Open-Drain Bidirectional Data	GPIO2 GPIO14 GPIO17 GPIO25 GPIO34 GPIO40	GPIO2 GPIO14 GPIO17 GPIO25 GPIO34 GPIO47	GPIO2 GPIO17	GPIO2 GPIO17
UARTA_RX	I	UART-A Receive Data	GPIO3 GPIO9 GPIO17 GPIO25 GPIO28 GPIO35/TDI	GPIO3 GPIO9 GPIO17 GPIO25 GPIO28 GPIO35/TDI GPIO49	GPIO3 GPIO9 GPIO17 GPIO28 GPIO35/TDI	GPIO3 GPIO9 GPIO17 GPIO28 GPIO35/TDI
UARTA_TX	O	UART-A Transmit Data	GPIO2 GPIO8 GPIO16 GPIO24	GPIO2 GPIO8 GPIO16 GPIO24	GPIO2 GPIO8 GPIO16 GPIO24	GPIO2 GPIO8 GPIO16 GPIO24

Signal name	Pin type	Description	LQFP100	LQFP80	LQFP64	QFN56
			GPIO29 GPIO37/TDO	GPIO29 GPIO37/TDO	GPIO29 GPIO37/TDO	GPIO29 GPIO37/TDO
UARTB_RX	I	UART-B Receive data	GPIO11 GPIO13 GPIO15 GPIO23 GPIO53 GPIO57	GPIO11 GPIO13 GPIO15 GPIO23 GPIO41 GPIO43 GPIO53	GPIO11 GPIO13 GPIO23	GPIO11 GPIO13 GPIO2
UARTB_TX	O	UART-B Transmit Data	GPIO9 GPIO10 GPIO12 GPIO14 GPIO18_X2 GPIO22 GPIO40 GPIO54 GPIO56	GPIO9 GPIO10 GPIO12 GPIO14 GPIO18_X2 GPIO22 GPIO42 GPIO54	GPIO9 GPIO10 GPIO12 GPIO18_X2 GPIO22	GPIO9 GPIO12 GPIO18_X2 GPIO22
SD1_C1	I	SDF-1 Channel 1 Clock Input	GPIO17 GPIO25	GPIO17 GPIO25 GPIO49	GPIO17	GPIO17
SD1_C2	I	SDF-1 Channel 2 Clock Input	GPIO27	GPIO27		
SD1_C3	I	SDF-1 Channel 3 Clock Input	GPIO29 GPIO33 GPIO53 GPIO57	GPIO29 GPIO33 GPIO53	GPIO29 GPIO33	GPIO29 GPIO33
SD1_C4	I	SDF-1 Channel 4 Clock Input	GPIO23 GPIO31	GPIO23 GPIO31	GPIO23	GPIO23

Signal name	Pin type	Description	LQFP100	LQFP80	LQFP64	QFN56
			GPIO59			
SD1_D1	I	SDF-1 Channel 1 Data Input	GPIO16 GPIO24	GPIO16 GPIO24	GPIO16 GPIO24	GPIO16 GPIO24
SD1_D2	I	SDF-1 Channel 2 Data Input	GPIO18_X2 GPIO26	GPIO18_X2 GPIO26	GPIO18_X 2	GPIO18_X 2
SD1_D3	I	SDF-1 Channel 3 Data Input	GPIO28 GPIO32 GPIO56	GPIO28 GPIO32	GPIO28 GPIO32	GPIO28 GPIO32
SD1_D4	I	SDF-1 Channel 4 Data Input	GPIO22 GPIO30 GPIO54 GPIO58	GPIO22 GPIO30 GPIO54	GPIO22	GPIO22
SPIA_CLK	I/O	SPI-A Clock	GPIO3 GPIO9 GPIO12 GPIO18_X2 GPIO56	GPIO3 GPIO9 GPIO12 GPIO18_X2	GPIO3 GPIO9 GPIO12 GPIO18_X2	GPIO3 GPIO9 GPIO12 GPIO18_X2
SPIA_SIMO	I/O	SPI-A Slave Input, Master Output	GPIO2 GPIO8 GPIO11 GPIO16 GPIO54	GPIO2 GPIO8 GPIO11 GPIO16 GPIO54	GPIO2 GPIO8 GPIO11 GPIO16	GPIO2 GPIO8 GPIO11 GPIO16
SPIA_SOMI	I/O	SPI-A Slave Output, Master Input	GPIO1 GPIO10 GPIO13 GPIO17	GPIO1 GPIO10 GPIO13 GPIO17	GPIO1 GPIO10 GPIO13 GPIO17	GPIO1 GPIO17 GPIO13
SPIA_STE	I/O	SPI-A Slave Transmit Enable	GPIO0 GPIO5	GPIO0 GPIO5	GPIO0 GPIO5	GPIO0 GPIO5

Signal name	Pin type	Description	LQFP100	LQFP80	LQFP64	QFN56
			GPIO11 GPIO57	GPIO11	GPIO11	GPIO11
SPIB_CLK	I/O	SPI-B Clock	GPIO4 GPIO12 GPIO14 GPIO22 GPIO26 GPIO28 GPIO32 GPIO58	GPIO4 GPIO14 GPIO22 GPIO26 GPIO28 GPIO32	GPIO4 GPIO12 GPIO22 GPIO23 GPIO28 GPIO32	GPIO4 GPIO12 GPIO22 GPIO23 GPIO28 GPIO32
SPIB_SIMO	I/O	SPI-B Slave Input, Master Output	GPIO7 GPIO23 GPIO24 GPIO30 GPIO56	GPIO7 GPIO23 GPIO24 GPIO30 GPIO47	GPIO7 GPIO23 GPIO24	GPIO7 GPIO23 GPIO24
SPIB_SOMI	I/O	SPI-B Slave Output, Master Input	GPIO6 GPIO16 GPIO25 GPIO31 GPIO57	GPIO6 GPIO16 GPIO25 GPIO31 GPIO41	GPIO6 GPIO16	GPIO6 GPIO16
SPIB_STE	I/O	SPI-B Slave Transmit Enable	GPIO15 GPIO23 GPIO27 GPIO29 GPIO33 GPIO53 GPIO59	GPIO15 GPIO23 GPIO27 GPIO29 GPIO33 GPIO41 GPIO53	GPIO23 GPIO29 GPIO33	GPIO23 GPIO29 GPIO33
SYNCOUT	O	External PWM Synchronization	GPIO6	GPIO6	GPIO6	GPIO6

Signal name	Pin type	Description	LQFP100	LQFP80	LQFP64	QFN56
		Pulse		GPIO49		
TDI	I	JTAG test data input. By default, the internal pull-up resistor is disabled. If this pin is used as JTAG TDI, the internal pull-up resistor should be enabled or an external pull-up resistor should be added on the circuit board to avoid input suspension	GPIO35/TDI	GPIO35/TDI	GPIO35/TDI	GPIO35/TDI
TDO	O	JTAG Test Data Output. By default, the internal pull-up resistor is disabled. When there is no JTAG activity, the TDO function will be under a three-state condition, causing this pin to be suspended; the internal pull-up resistor should be enabled or an external pull-up resistor should be added on the circuit board to avoid GPIO input suspension.	GPIO37/TDO	GPIO37/TDO	GPIO37/TDO	GPIO37/TDO
X1	I	Crystal Oscillator Input	X1	X1	X1	X1
X2	O	Crystal Oscillator Output	GPIO18_X2	GPIO18_X2	GPIO18_X2	GPIO18_X2
XCLKOUT	O	External Clock Output. This pin outputs the frequency division version of the selected clock signals from the devices.	GPIO16 GPIO18_X2	GPIO16 GPIO18_X2	GPIO16 GPIO18_X2	GPIO16 GPIO18_X2

3.4.2. Digital Input on ADC Pin (AIO)

GPIO (GPO224-GPIO254) on Port H is multiplexed with analog pins. This is also known as AIO. These pins can only operate in input mode. By default, these pins will be used as analog pins, and GPIO will be in a high-impedance state. The GPHAMSEL register is used to configure the digital or analog operations of these pins.

Note: If a digital signal with sharp edges (high dv/dt) is connected to AIO, crosstalk may occur to the adjacent analog signals. Therefore, if the adjacent channels are used for analog function, users should limit the edge rate of signals connected to AIO.

3.4.3. GPIO Input X-BAR

Input X-BAR is used to route signals from GPIO to many different IP blocks, for example ADC, CAP, PWM, and external interrupts.

Figure 5 Input X-BAR

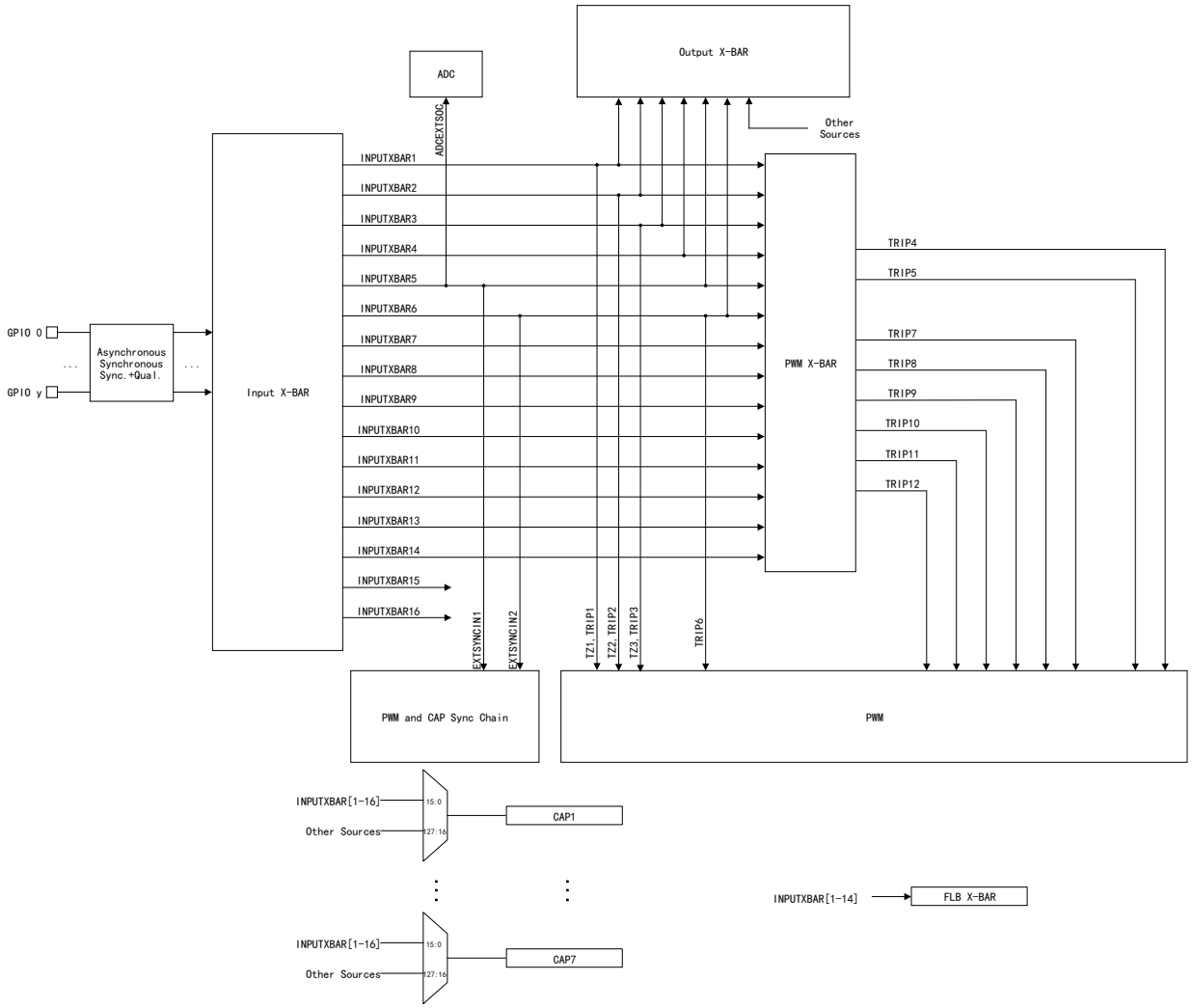


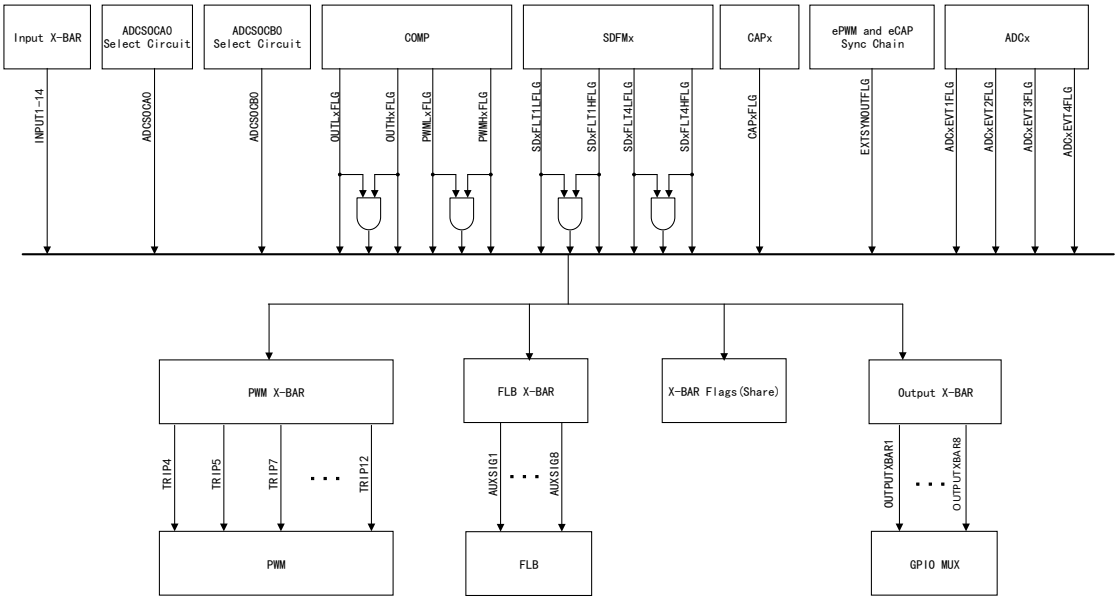
Table 10 Input X-BAR Target

Input	Target
Input 1	CAPx, PWM X-BAR, PWM[TZ1, TRIP1], Output X-BAR
Input 2	CAPx, PWM X-BAR, PWM[TZ2, TRIP2], Output X-BAR
Input 3	CAPx, PWM X-BAR, PWM[TZ3, TRIP3], Output X-BAR
Input 4	CAPx, PWM X-BAR, XINT1, Output X-BAR
Input 5	CAPx, PWM X-BAR, XINT2, ADCEXTSOC, EXTSYNCIN1, Output X-BAR
Input 6	CAPx, PWM X-BAR, XINT3, PWM[TRIP6], EXTSYNCIN2, Output X-BAR
Input 7	CAPx, PWM X-BAR
Input 8	CAPx, PWM X-BAR
Input 9	CAPx, PWM X-BAR
Input 10	CAPx, PWM X-BAR
Input 11	CAPx, PWM X-BAR
Input 12	CAPx, PWM X-BAR
Input 13	CAPx, PWM X-BAR, XINT4
Input 14	CAPx, PWM X-BAR, XINT5
Input 15	CAPx
Input 16	CAPx

3.4.4. Output X-BAR and PWM X-BAR

The output X-BAR has eight outputs, which are routed to GPIO modules. PWM X-BAR has eight outputs, which are routed to each PWM module.

Figure 6 Output X-BAR and PWM X-BAR Sources



3.5. Pins with Internal Pull-up or Pull-down Resistor

Some pins on the device have internal pull-up or pull-down resistor. The pulling direction and its activity time are listed in the following table. By default, the pull-up resistor of GPIO pins is disabled and can be enabled through software. To avoid any suspending unbound inputs, Boot ROM will enable internal pull-up resistor for unbound GPIO pins in specific package. Other pins with pull-up and pull-down resistors mentioned in the following table are always in enabled state and cannot be disabled.

Table 11 Pins with Internal Pull-up and Pull-down Resistors

Pin	Reset (XRSn=0)	Device guidance	Application
GPOx (including AIO)	Disable pull-up resistor	Disable pull-up resistor (1)	Application definition
GPIO35/TDI	Disable pull-up resistor		Application definition
GPIO37/TDO	Disable pull-up resistor		Application definition
TCK	The pull-up resistor is effective		
TMS	The pull-up resistor is effective		
VREGENZ	The pull-down resistor is effective		
XRSn	The pull-up resistor is effective		
Other pins	The pull-up or pull-down resistor does not exist		

Note: The unbound pins in the given package will have internal pull-up resistor enabled by Boot ROM.

3.6. Connection of Unused Pins

For applications that do not need to use all functions of the device, the acceptable conditions for any unused pins are listed in the following table. When multiple options are listed, any option is acceptable.

Table 12 Connection of Unused Pins

Signal name	Acceptable practice
Analog	
Analog input pin with DACx_OUT	No connection Connect to VSSA through a resistor of 4.7kΩ or greater
Analog input pins (except for DACx_OUT)	No connection Bound to VSSA Connect to VSSA through a resistor
VREFHIx	Connect to VDDA (only applicable when ADC or DAC is not used in the application)
VREFLOx	Bound to VSSA
Digital	
GPIOx	No connection (enable the input mode of internal pull-up resistor) No connection (disable the output mode of internal pull-up resistor) Pull-up or pull-down resistor (resistor of any value, input mode, disable internal pull-up resistor)
GPIO35/TDI	When selecting the TDI multiplexer option (default), GPIO is in input mode. Enable the internal pull-up resistor External pull-up resistor
GPIO37/TDO	When the TDO multiplexing option is selected (default), GPIO is in output mode only during JTAG activity; otherwise, it is in a three-state condition. This pin must be biased to avoid generating extra current on the input buffer. Enable the internal pull-up resistor External pull-up resistor
TCK	No connection Pull-up resistor
TMS	Pull-up resistor
VREGENZ	Connected to VSS
X1	Connected to VSS
GPIO18/X2	Turn off XTAL and: Enable the input mode of internal pull-up resistor External pull-up or pull-down resistor (input mode) Disable the output mode of internal pull-up resistor
Power supply and grounding	
V_{DD}	All VDD pins must be connected as described in "Pin Signal Description".
V_{DDA}	If no dedicated analog power supply is used, connect to VDDIO.
VDDIO	All VDDIO pins must be connected as described in "Pin Signal Description".
VSS	All VSS pins must be connected to the circuit board ground.
VSSIO	Always connect to VSS.
VSSA	If analog grounding is not used, connect to VSS.

4. Module Description

4.1. Introduction

G32R501x is a high-performance MCU developed by Geehy for real-time control applications. It is equipped with a Arm® Cortex® -M52 microprocessor based on the Arm® v8.1-M architecture and supports up to 2 cores. The cores can work in parallel and collaborate efficiently, so it is suitable for such applications as motion control, photovoltaic inverters, digital power supplies, and on-board chargers (OBC).

The maximum operating frequency of G32R5xx MCU can be up to 250MHz, realizing custom data path extension (CDE) for Arm® Rv8-M. It is equipped with Helium™ technology based on vector extension scheme (MVE), which further improves the processing performance through innovative Zidian Math Instruction Extension. The Zidian Math Instruction Extension can quickly execute the algorithms that include the common trigonometric operations in transformation and torque loop calculation, and reduce the delay of common complex mathematical operation in coding application.

G32R5xx supports up to 640KB Flash internally. The Flash is divided into two independent memory banks of 512KB and 128KB, supporting parallel programming and execution. Besides, through the built-in CFGSMS, it can implement efficient system partitioning for 128KB SRAM storage on the chip. Each logical block has a size of 8KB, which can be configured for different types of usage, e.g. ITCM, DTCM, and SRAM. In addition, G32R5xx also supports Flash ECC, RAM parity, and security attribute configuration.

G32R5xx chip integrates high-performance analog unit, which can further improve the system control performance. Three independent 12-bit ADC can accurately and efficiently collect and process multiple analog signals, thereby improving system throughput. 7 comparator subsystems can constantly monitor the input voltage level through the tripping function.

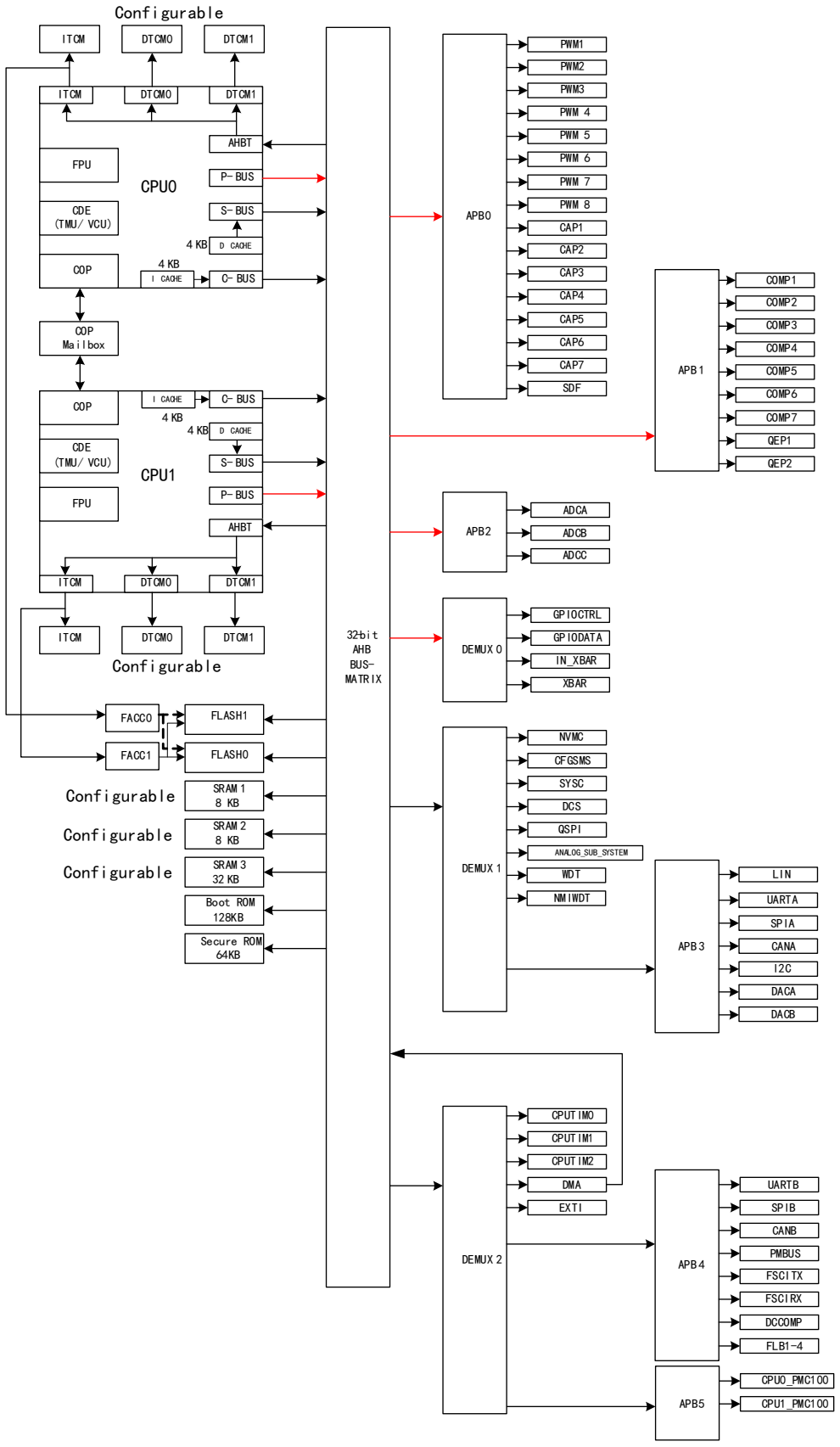
G32R5xx includes performance-leading control peripherals (with frequency-independent PWM and CAP/HRCAP), which can place excellent control over the system. The built-in 4-channel SDF is suitable for external isolated Σ-Δ modulators.

Universal communication ports (e.g. SPI, UART, I2C, LIN, and CAN) are built in G32R5xx, and multiple multiplexing options are provided to meet the communication requirements of various applications. The G32R5xx device also provides the PMBus interface and high-speed QSPI interface that fully comply with the standards. Besides, G32R5xx also supports JTAG, cJTAG, and SWD debugging interfaces. The multiple debugging modes are suitable for different system environments and performance requirements.

G32R5xx supports the operating temperatures ranging from -40℃ to 105℃/125℃, and provides multiple packages for selection such as QFN56, LQFP64, LQFP80, and LQFP100.

4.2. Functional Block Diagram

Figure 7 Functional Block Diagram



Note:

(1) The red lines in the figure represent bus bridge.

(2) The size of ITCM/DTCM/SRAM is configured using CFGSMS.

4.3. Memory

4.3.1. Memory mapping

The memory mapping is shown in the table below.

Table 13 Memory Mapping

Address range (Hex)	Size (Max)	Description
0x0000_0000 – 0x0001_FFFF	128KB	CPU0 ITCM (64KB for single-core version, and 48KB for dual-core version by default)
0xA000_0000 – 0xA001_FFFF	128KB	CPU0 ITCM (CPU0-AHBT) (64KB for single-core version, and 48KB for dual-core version by default)
0x0000_0000 – 0x0001_FFFF	128KB	CPU1 ITCM (0KB for single-core version, and 8KB for dual-core version by default)
0xA100_0000 – 0xA101_FFFF	128KB	CPU1 ITCM (CPU1-AHBT) (0KB for single-core version, and 8KB for dual-core version by default)
0x0008_0000 – 0x0008_BFFF	48KB	FLASH INFO on ITCM
0x0009_0000 – 0x0009_3FFF	16KB	FLASH INFO1 on ITCM
0x0010_0000 - 0x0019_FFFF	640KB	FLASH memory on ITCM
0x0800_0000 - 0x0809_FFFF	640KB	FLASH memory on BUSMATRIX
0x0810_0000 - 0x0810_BFFF	48KB	FLASH INFO on BUSMATRIX
0x0818_0000 - 0x0818_3FFF	16KB	FLASH INFO1 on BUSMATRIX
0x0900_0000 - 0x0901_FFFF	128KB	FLASH ECC
0x1000_0000 – 0x1001_FFFF	128KB	Boot ROM
0x1002_0000 – 0x1002_FFFF	64KB	Secure ROM
0x2000_0000 - 0x2001_FFFF	128KB	CPU0 DTCM (16KB for single-core version, and 16KB for dual-core version by default)
0xA010_0000 - 0xA011_FFFF	128KB	CPU0 DTCM (CPU0-AHBT) (16KB for single-core version, and 16KB for dual-core version by default)
0x2000_0000 – 0x2001_FFFF	128KB	CPU1 DTCM (0KB for single-core version, and 8KB for dual-core version by default)
0xA110_0000 - 0xA111_FFFF	128KB	CPU1 DTCM (CPU1-AHBT) (0KB for single-core version, and 8KB for dual-core version by default)

Address range (Hex)	Size (Max)	Description
0x2010_0000 - 0x2011_FFFF	128KB	SRAM1 (Default 8KB)
0x2020_0000 - 0x2021_FFFF	128KB	SRAM2 (Default 8KB)
0x2030_0000 - 0x2031_FFFF	128KB	SRAM3 (Default 32KB)
Address range (Hex)	Bus	Function
0x4000_0000 – 0x4000_FFFF	APB0	APB peripherals
0x4001_0000 – 0x4001_FFFF	APB1	APB peripherals
0x4002_0000 – 0x4002_FFFF	APB2	APB peripherals
0x4003_0000 – 0x4003_FFFF	DEMUX0	AHB peripherals
0x5000_0000 – 0x5000_FFFF	APB3	APB peripherals
0x5000_0000 – 0x5002_FFFF	DEMUX1	AHB peripherals
0x6000_0000 – 0x6FFF_FFFF		
0x5010_0000 – 0x5010_3FFF	APB4	APB peripherals
0x5010_4000 – 0x5010_FFFF	APB5	APB peripherals
0x5010_0000 – 0x5011_FFFF	DEMUX2	AHB peripherals

4.3.2. FLASH mapping

Up to two Flash memory banks (128KB for Bank0 and 512KB for Bank1) can be used on the G32R5xx device. The Flash memory banks are controlled by two NVMC (nonvolatile memory controllers). Both CPU0 and CPU1 can access FLASH MEM through ITCM/C-BUS. The physical storage space accessed by two paths is the same, but the address is different. All FLASH erase/write operations are performed by operating the NVMC register. The FLASH MEM area address is read-only for CPU0/1 and DMA, and all write operations will be ignored. Any type of access should not be made to the Flash memory banks that are performing erasing/programming operations.

Table 14 Flash Sector Address (configured according to memory single bank (256 bits of reading width))

IP	Name	Sector base on C-BUS interface	Sector base on ITCM interface	Sector size	Bank number
Main memory	Sector0	0x0800_0000~0x0800_3FFF	0x0010_0000~0x0010_3FFF	16KByte	Bank0 & Bank1 mix
	Sector1	0x0800_4000~0x0800_7FFF	0x0010_4000~0x0010_7FFF	16KByte	Bank0 & Bank1 mix
	Sector2	0x0800_8000~0x0800_BFFF	0x0010_8000~0x0010_BFFF	16KByte	Bank0 & Bank1 mix
	.....	.....	.....	.....	Bank0 & Bank1 mix
	Sector14	0x0803_8000~0x0803_BFFF	0x0013_8000~0x0013_BFFF	16KByte	Bank0 & Bank1 mix
	Sector15	0x0803_C000~0x0803_FFFF	0x0013_C000~0x0013_FFFF	16KByte	Bank0 & Bank1 mix

IP	Name	Sector base on C-BUS interface	Sector base on ITCM interface	Sector size	Bank number
	Sector16	0x0804_0000~0x0804_1FFF	0x0014_0000~0x0014_1FFF	8KByte	Bank1
	…….	…….	…….	…….	Bank1
	Sector63	0x0809_E000~0x0809_FFFF	0x0019_E000~0x0019_FFFF	8KByte	Bank1
IFREN	Bank0 back-up sector0	0x0810_0000~0x0810_1FFF	0x0008_0000~0x0008_1FFF	8Kbyte	Bank0
	Bank0 back-up sector1	0x0810_2000~0x0810_3FFF	0x0008_2000~0x0008_3FFF	8Kbyte	Bank0
	Bank0 back-up sector2	0x0810_4000~0x0810_5FFF	0x0008_4000~0x0008_5FFF	8KByte	Bank0
	Bank0 back-up sector3	0x0810_6000~0x0810_7FFF	0x0008_6000~0x0008_7FFF	8KByte	Bank0
	Bank1 User Option byte	0x0810_8000~0x0810_9FFF	0x0008_8000~0x0008_9FFF	8Kbyte	Bank1
	Bank1 OTP	0x0810_A000~0x0810_BFFF	0x0008_A000~0x0008_BFFF	8Kbyte	Bank1
IFREN1	FLASH trimming	0x0818_0000~0x0818_3FFF	0x0009_0000~0x0009_3FFF	16KByte	Bank0 & Bank1 mix
	ECC	0x0900_0000~0x0902_17FF	NA	128Kbyte (half-word access only)	Bank0 & Bank1 mix

Table 15 Flash Sector Address (configured according to memory dual bank (128 bits of reading width))

IP	Name	Sector base on C-BUS interface	Sector base on ITCM interface	Sector size	Bank number
Main memory bank0	Sector0	0x0800_0000~0x0800_1FFF	0x0010_0000~0x0010_1FFF	8KByte	Bank0
	Sector1	0x0800_2000~0x0800_3FFF	0x0010_2000~0x0010_3FFF	8KByte	Bank0
	Sector2	0x0800_4000~0x0800_5FFF	0x0010_4000~0x0010_5FFF	8KByte	Bank0
	…….	…….	…….	…….	Bank0
	Sector14	0x0801_C000~0x0801_DFFF	0x0011_C000~0x0011_DFFF	8KByte	Bank0

IP	Name	Sector base on C-BUS interface	Sector base on ITCM interface	Sector size	Bank number
	Sector15	0x0801_E000~0x0801_FFFF	0x0011_E000~0x0011_FFFF	8KByte	Bank0
Main memory bank1	Sector16	0x0802_0000~0x0802_1FFF	0x0012_0000~0x0012_1FFF	8KByte	Bank1
	Sector17	0x0802_2000~0x0802_3FFF	0x0012_2000~0x0012_3FFF	8KByte	Bank1
	Sector18	0x0802_4000~0x0802_5FFF	0x0012_4000~0x0012_5FFF	8Kbyte1	Bank1
	…….	…….	…….	…….	Bank1
	Sector30	0x0803_C000~0x0803_DFFF	0x0013_C000~0x0013_DFFF	8KByte	Bank1
	Sector31	0x0803_E000~0x0803_FFFF	0x0013_E000~0x0013_FFFF	8KByte	Bank1
	Sector32	0x0804_0000~0x0804_1FFF	0x0014_0000~0x0014_1FFF	8KByte	Bank1
	…….	…….	…….	…….	Bank1
	Sector79	0x0809_E000~0x0809_FFFF	0x0019_E000~0x0019_FFFF	8KByte	Bank1
IFREN	Bank0 back-up sector0	0x0810_0000~0x0810_1FFF	0x0008_0000~0x0008_1FFF	8Kbyte	Bank0
	Bank0 back-up sector1	0x0810_2000~0x0810_3FFF	0x0008_2000~0x0008_3FFF	8Kbyte	Bank0
	Bank0 back-up sector2	0x0810_4000~0x0810_5FFF	0x0008_4000~0x0008_5FFF	8KByte	Bank0
	Bank0 back-up sector3	0x0810_6000~0x0810_7FFF	0x0008_6000~0x0008_7FFF	8KByte	Bank0
	Bank1 User Option byte	0x0810_8000~0x0810_9FFF	0x0008_8000~0x0008_9FFF	8Kbyte	Bank1
	Bank1 OTP	0x0810_A000~0x0810_BFFF	0x0008_A000~0x0008_BFFF	8Kbyte	Bank1
IFREN1	FLASH trimming	0x0818_0000~0x0818_3FFF	0x0009_0000~0x0009_3FFF	16KByte	Bank0 & Bank1 mix
	ECC	0x0900_0000~0x0902_17FF	NA	128Kbyte (half-word access only)	Bank0 & Bank1 mix

4.3.3. Peripheral register memory mapping

Table 16 Peripheral Register Memory Mapping

Address	Bus	IP
0x4000_0000-0x4000_03FF	APB0	PWM1
0x4000_0400-0x4000_07FF		PWM2
0x4000_0800-0x4000_0BFF		PWM3

Address	Bus	IP
0x4000_0C00-0x4000_0FFF		PWM4
0x4000_1000-0x4000_13FF		PWM5
0x4000_1400-0x4000_17FF		PWM6
0x4000_1800-0x4000_1BFF		PWM7
0x4000_1C00-0x4000_1FFF		PWM8
0x4000_2000-0x4000_23FF		CAP1
0x4000_2400-0x4000_27FF		CAP2
0x4000_2800-0x4000_2BFF		CAP3
0x4000_2C00-0x4000_2FFF		CAP4
0x4000_3000-0x4000_33FF		CAP5
0x4000_3400-0x4000_37FF		CAP6
0x4000_3800-0x4000_3BFF		CAP7
0x4000_3C00-0x4000_3FFF		SDF
0x4000_4000-0x4000_FFFF		Reserved
0x4001_1C00-0x4001_1FFF	APB1	COMP1
0x4001_2000-0x4001_23FF		COMP2
0x4001_2400-0x4001_27FF		COMP3
0x4001_2800-0x4001_2BFF		COMP4
0x4001_2C00-0x4001_2FFF		COMP5
0x4001_3000-0x4001_33FF		COMP6
0x4001_3400-0x4001_37FF		COMP7
0x4001_3800-0x4001_3BFF		QEP1
0x4001_3C00-0x4001_3FFF		QEP2
0x4001_4000-0x4001_FFFF		Reserved
0x4002_0000-0x4002_03FF	APB2	ADCA
0x4002_0400-0x4002_07FF		ADCB
0x4002_0800-0x4002_0BFF		ADCC
0x4002_0C00-0x4002_FFFF		Reserved
0x4003_0000-0x4003_07FF	DEMUX0	GPIOCTRL
0x4003_0800-0x4003_0BFF		GPIODATA
0x4003_0C00-0x4003_0C7F		INPUTXBAR
0x4003_0C80-0x4003_0FFF		SyncSocREG
0x4003_1000-0x4003_103F		XBAR_REG

Address	Bus	IP
0x4003_11C0-0x4003_123F		PWM_XBAR_REG
0x4003_1240-0x4003_12BF		FLB_XBAR_REG
0x4003_12C0-0x4003_133F		OUTPUT_XBAR_REG
0x4003_1400-0x4003_FFFF		Reserved
0x5000_0000-0x5000_03FF	APB3	LIN
0x5000_0400-0x5000_0BFF		Reserved
0x5000_0C00-0x5000_0FFF		UARTA
0x5000_1000-0x5000_13FF		SPIA
0x5000_1400-0x5000_17FF		I2C
0x5000_1800-0x5000_1BFF		DACA
0x5000_1C00-0x5000_1FFF		DACB
0x5000_2000-0x5000_27FF		CANA
0x5000_2800-0x5000_FFFF		Reserved
0x5000_0000-0x5000_FFFF	DEMUX1	APB3
0x5001_0000-0x5001_07FF		NVMC
0x5001_0800-0x5001_0BFF		CFGSMS
0x5001_0C00-0x5001_FFFF		Reserved
0x5002_0000-0x5002_3FFF		SYSC
0x5002_4000-0x5002_5FFF		DCS
0x5002_6000-0x5002_63FF		QSPI
0x5002_6400-0x5002_64BF		WWDT
0x5002_64C0-0x5002_67FF		NMIWDT
0x5002_6800-0x5002_7FFF		Reserved
0x5002_8000-0x5002_83FF		ANALOG_SUB_SYSTEM
0x5002_8400-0x5002_FFFF		Reserved
0x6000_0000-0x6FFF_FFFF		QSPI_MEMORY
0x5010_0000-0x5010_03FF	APB4	UARTB
0x5010_0400-0x5010_07FF		SPIB
0x5010_0800-0x5010_0BFF		PMBUS
0x5010_0C00-0x5010_0FFF		Reserved
0x5010_1000-0x5010_13FF		Reserved
0x5010_1400-0x5010_17FF		DCC
0x5010_1800-0x5010_1FFF		CANB

Address	Bus	IP
0x5010_2000-0x5010_27FF		FLB1
0x5010_2800-0x5010_2FFF		FLB2
0x5010_3000-0x5010_37FF		FLB3
0x5010_3800-0x5010_3FFF		FLB4
0x5010_0000-0x5010_3FFF	DEMUX2	APB4
0x5010_4000-0x5010_FFFF		APB5
0x5011_0000-0x5011_03FF		TMR0
0x5011_0400-0x5011_07FF		TMR1
0x5011_0800-0x5011_0BFF		TMR2
0x5011_0C00-0x5011_0FFF		DMA
0x5011_1000-0x5011_13FF		EXTI
0x5011_1400-0x5011_FFFF		Reserved

4.3.4. Memory types

4.3.4.1. RAM (ITCM, DTCM, SRAM)

Through the built-in CFGSMS, the G32R5xx device can implement efficient system partitioning for 128KB SRAM storage on the chip. Each logical block has a size of 8KB, which can be configured for different types of usage, e.g. ITCM, DTCM, and SRAM.

The CPU subsystems have two small non-secure blocks ITCM and DTCM that are closely coupled to CPU (i.e. only CPU can access these memories). In addition, G32R5xx also supports RAM parity check function.

4.4. Identification

The following table lists the device identification registers. Please refer to PARTIDH and PARTIDL register description for availability of identification of mass production status and other device information.

Table 17 Device Identification Registers

Name	Address	Size (x8)	Description	
PARTIDH	0x5002 0514	4	Identification number of device model G32R501	0x01FF 0500
REVID	0x5002 0518	4	Device revision number Revision 0	0x0000 0000
UID_UNIQUE	0x0810 AF88	4	Unique identification number. This number is different on each individual device with the same PARTIDH.	

Name	Address	Size (x8)	Description
			This unique number can be used as the serial number in application.

4.5. Bus Architecture - Peripheral Connection

Table 18 Access of Main Devices of the Bus to Peripherals

Peripheral	DMA	CPU0	CPU1
System peripherals			
CPU timer		Supported	Supported
System configuration (WDT, NMIWDT, LPM, peripheral clock gating)		Supported	Supported
Device function, peripheral reset		Supported	Supported
Clock and PLL configuration		Supported	Supported
Flash configuration		Supported	Supported
Reset configuration		Supported	Supported
GPIO pin mapping and configuration		Supported	Supported
GPIO data (1)		Supported	Supported
DMA trigger source selection		Supported	Supported
Control peripherals			
PWM/HRPWM	Supported	Supported	Supported
CAP/HRCAP	Supported	Supported	Supported
QEP（2）	Supported	Supported	Supported
SDF	Supported	Supported	Supported
Analog peripherals			
Analog system control		Supported	Supported
ADC configuration	Supported	Supported	Supported
ADC result (3)	Supported	Supported	Supported
COMP（2）	Supported	Supported	Supported
DAC（2）	Supported	Supported	Supported
Communication peripherals			
CAN	Supported	Supported	Supported
SPI	Supported	Supported	Supported
QSPI	Supported	Supported	Supported
I2C		Supported	Supported
PMBus	Supported	Supported	Supported
UART		Supported	Supported
LIN	Supported	Supported	Supported

Note:

(1) GPIO data registers are unique to the CPU. When the GPIO pin mapping register is configured to assign GPIO to a specific master device, this GPIO will be controlled by the corresponding GPIO data register.

(2) These modules can be accessed through DMA, but cannot trigger DMA transmission.

(3) The ADC result register of each master device is repeated. This enables them to be read in a 0 wait state without the need for arbitration of any or all master devices.

4.6. Processor

G32R5xx integrates Arm® Cortex-M52 core. Two cores can work in parallel to perform high-performance computing tasks while executing real-time control tasks. Cortex-M52 is a second-generation "Star" series embedded processor launched by Arm China. Based on the latest Arm® v8.1-M architecture design, it is the first locally developed vehicle-grade embedded processor that supports functional security design. It not only has stronger AI and DSP processing capability, higher computing density and energy efficiency ratio, but also focuses on optimizing the functional safety and information security required for the Internet of Things and on-board equipment.

4.6.1. Floating point unit (FPU)

The Cortex-M52 processor FPU provides scalar half-precision, single-precision, and double-precision floating-point operations. FPU supports addition, subtraction, multiplication, division, product, and square root operations, and can provide conversions between fixed-point and floating-point data formats, as well as floating-point constant instructions.

The Cortex-M52 processor provides floating-point computing capability, including floating-point extension, conforming to ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic.

4.6.2. Triangular mathematical unit (TMU)

TMU extends the functions of Cortex-M52 + FPU by adding instructions and utilizing the existing FPU instructions that can accelerate the execution of common trigonometric functions and the arithmetic operations listed in the table below.

Table 19 Name Mapping of FCAU Assembly Instructions

Arm® assembly instruction	Assembly instruction renamed in “Zidian_cde.h”	Performance: Execution cycle
VCX2 0, Sd, Sm, #0x0	SINPUF32 Sd, Sm.	2
VCX2 0, Sd, Sm, #0x1	COSPUF32 Sd, Sm.	2
VCX2 0, Sd, Sm, #0x2	ATANPUF32 Sd, Sm.	2
VCX2 0, Sd, Sm, #0x3	MPY2PIF32 Sd, Sm.	1
VCX2 0, Sd, Sm, #0x4	DIV2PIF32 Sd, Sm.	1
VCX2 0, Sd, Sm, #0x5	SQRTF32 Sd, Sm.	2
VCX2 0, Sd, Sm, #0x6	RD_SCR Sd, Sm.	1
VCX2 0, Sd, Sm, #0x7	WR_SCR Sd, Sm.	1

Arm® assembly instruction	Assembly instruction renamed in “Zidian_cde.h”	Performance: Execution cycle
VCX3 0, Sd, Sn, Sm, #0x0	DIVF32 Sd, Sn, Sm.	2
VCX3 0, Sd, Sn, Sm, #0x1	QUADF32 Sd, Sn, Sm.	1
VCX3 0, Sd, Sn, Sm, #0x2	DIVF32_ATAN2 Sd, Sn, Sm.	2

Arm® Cortex® -M52 FPU assembly instructions are difficult for users to understand because they do not include any information about instruction behavior. Therefore, the original G32R501 FPU assembly instructions have been renamed, and all the renamed assembly instructions are included in “zidian_cde.h.”

4.6.3. Viterbi, complex mathematics, and CRC Unit (VCU)

The Cortex-M52 processor with VCU can extend the fixed-point or floating-point CPU functions by adding registers and instructions that support the following algorithm types.

4.6.3.1. Viterbi decoding

Viterbi decoding is usually used in baseband communication applications. The Viterbi decoding algorithm consists of three main parts: branch metric calculation, comparison-selection (Viterbi butterfly), and backtracking operation. The following table summarizes the VCU performance of each operation.

Table 20 Viterbi Decoding Performance

VITERBI operation	VCU cycle
Branch metric calculation (bit rate=1/2)	1
Branch metric calculation (bit rate=1/3)	2p
Viterbi butterfly (add-compare-select)	2 （1）
Backtracking at each stage	3（2）

Note:

(1) CPU takes 15 cycles to complete each butterfly.

(2) CPU takes 22 cycles to complete each stage.

4.6.3.2. Cyclic redundancy check (CRC)

CRC algorithm provides a simple method to verify integrity of data on large data blocks, communication data packets, or code segments. Cortex-M52+VCU can perform 8-bit, 16-bit, and 32-bit CRC. For example, VCU can calculate a CRC with a block length of 10 bytes within 10 cycles. The CRC result register contains the current CRC, which will be updated every time a CRC instruction is executed.

4.6.3.3. Complex mathematics

Complex mathematics is used in many applications, e.g.:

- Fast Fourier Transform (FFT): Used in spread spectrum communication and many signal processing algorithms.

- Complex filter: It can increase data reliability, extend transmission distance, and improve efficiency. Cortex-M52+VCU can multiply the complex numbers I and Q by the coefficients (four times) in a single cycle. In addition, Cortex-M52+VCU can read/write the real and imaginary parts of 16-bit complex data into the memory in a single cycle.

Table 21 Performance of Complex Mathematics

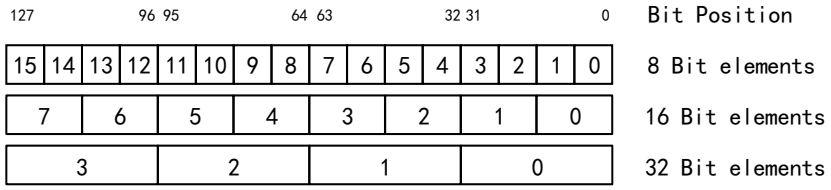
Operations of complex mathematics	VCU cycle	Precautions
Addition or subtraction	1	32 ± 32=32 bits (applicable to filters)
Addition or subtraction	1	16 ± 32=15 bits (applicable to FFT)
Multiplication	2p	16 × 16=32 bits
Multiplication and accumulation (MAC)	2p	32 + 32=32 bits, 16 × 16 = 32 bits
RPT MAC	2p+N	Repeat MAC. A single cycle after the first operation.

4.6.4. Helium

Helium™ technology is a vector extension scheme (MVE) for ARM Cortex-M processor series. It is part of the ARM v8.1-M architecture, enabling developers to improve the performance in DSP and machine learning applications. Helium™ Technology uses Single Instruction Multiple Data (SIMD) to perform the same operation on multiple data simultaneously, so as to provide optimized performance. MVE has two variants, i.e. integer and floating-point variants:

- MVE-I operates on 32-bit, 16 bit, and 8-bit data types, including Q7, Q15, and Q31.
- MVE-F operates on half-precision and single-precision floating-point values: MVE operation is orthogonally divided into two modes, i.e. channel and beat.
- The channel is part of the vector register or operation. The data placed in the channel is called an element. Multiple channels can be executed in each beat. Each vector instruction has four beats. The allowed channel width and channel operation per beat are:
  - For a 64-bit channel, half-channel operation is performed in one beat.
  - For a 32-bit channel, one-channel operation is performed in one beat.
  - For a 16-bit channel, two-channel operation is performed in one beat.
  - For a 8-bit channel, four-channel operation is performed in one beat.

Figure 8 Helium Vector Element Diagram



- The beat is a quarter of the MVE vector operation. As the length of the vector is 128 bits, one beat of the vector addition instruction is equivalent to computing a 32-bit result data. This is unrelated to the channel width. For example, if the channel width is

8 bits, one beat of the vector addition instruction will perform four 8-bit additions. The number of beats in each clock describes how many architecture statuses are updated by each architecture clock under normal circumstances. The system is classified as follows:

- In a single-beat system, each clock may produce one beat.
- In a double-beat system, each clock may produce two beats.
- In a four-beat system, each clock may produce four beats.

Cortex-M52 serves a double-beat system. It supports overlapping up to two-beat MVE instructions at any time, so that after one MVE instruction is issued, another MVE instruction can be issued without generating extra pauses. For more information, please refer to the Cortex-M52 Processor Device.

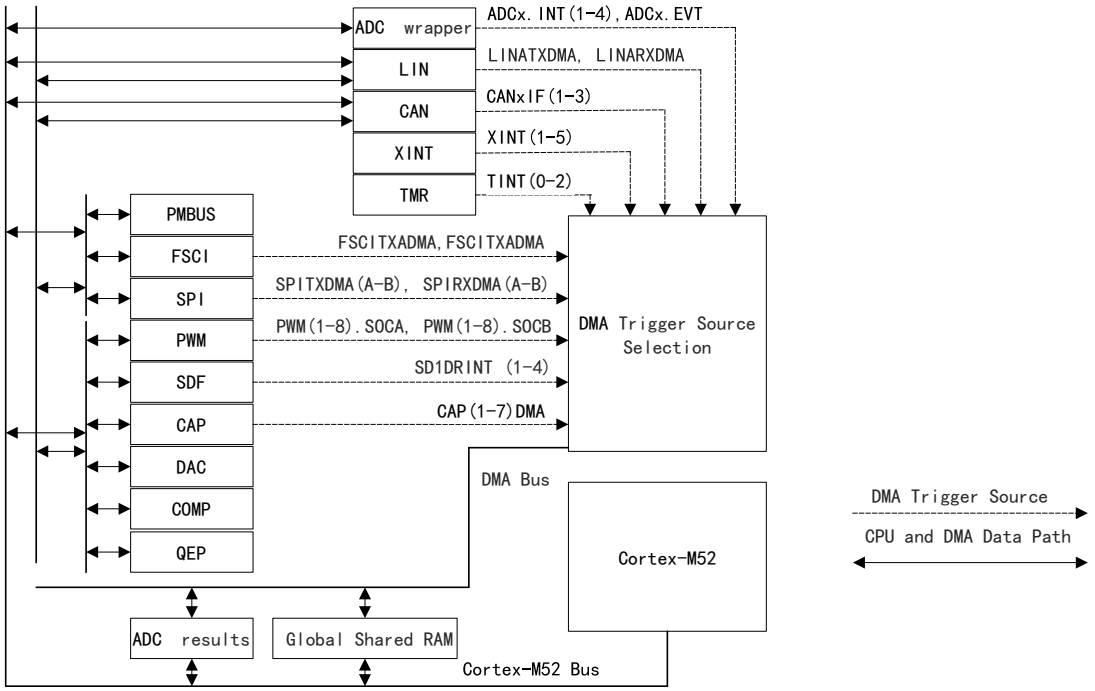
4.7. Direct Memory Access (DMA)

The DMA module provides a hardware method for transmitting data between peripherals and/or memory without CPU intervention, thereby releasing bandwidth for other system functions. Besides, DMA can perform orthogonal rearrangement during data transmission and perform "ping-pong" operation on data between buffers. These characteristics are very useful for structuring data into modules so as to optimize the CPU.

DMA characteristics include:

- Six channels with independent interrupts
- Peripheral interrupt trigger source
  - ADC interrupt and EVT signal
  - External Interrupt
  - PWM SOC signal
  - CPU timer
  - CAP
  - Σ- Δ filter module
  - SPI transmitting and receiving
  - CAN transmitting and receiving
  - LIN transmitting and receiving
  - QSPI transmitting and receiving
- Data source and target:
  - SRAM
  - FLASH
  - ADC result register
  - Control peripheral registers (PWM, QEP, CAP, SDF)
  - DAC
  - SPI, LIN, CAN, UART, I2C, and PMBus registers
- Word size: 16 bits or 32 bits (SPI is limited to 16 bits)
- Data rate: Four cycles per word, with no need for arbitration

Figure 9 DMA Structure Block Diagram



Description of DMA arbitration logic

DMA data transfer operates independently of CPU0 and CPU1. When DMA and CPU0, CPU1 simultaneously access an address, the arbitration logic will solve this conflict. The priority order for DMA, CPU0, and CPU1 to access any slave is DMA>CPU0>CPU1.

If CPU0 performs read and write operations while DMA executes write operation, the data written by DMA will be lost. Therefore, it is necessary to avoid performing write operation by CPU and DMA at the same time. Not applicable to DMA, CPU0, and CPU1 zero-wait access to ADC result registers.

4.8. Boot ROM and Peripheral Boot

G32R501 can select differet boot modes by changing the pin states of GPIO24 and GPIO32.

Table 22 Default Boot Mode

Boot mode	Default boot mode pins
UART/Wait for boot	GPIO24:0 and GPIO32:1
CAN	GPIO24:1 and GPIO32:0
Flash	GPIO24:1 and GPIO32:1

The possible boot modes supported on the device are listed in the following table. The default boot mode pins are GPIO24 (boot mode pin 1) and GPIO32 (boot mode pin 0). If users also use peripherals on these pins, the boot mode pin can be selected and set to weak pull-up, so the pull-up may be overdriven. On this device, customers can change the default boot mode pin by programming the user-configurable dual-code security module (DCS) OTP position.

Table 23 All Available Boot Modes

Boot mode number	Boot mode
1	UART/Wait for boot
2	CAN
3	Flash
4	Wait
5	RAM
6	SPI master
7	I2C master
10	Secure Flash

Note: All supported peripheral boot modes use the first instance of the peripheral module (UARTA, SPIA, I2CA, and CANA). All boot modes (e.g. UART boot) mentioned in this section actually refer to the first module instance, e.g. UART boot on UART port. This also applies to boot of other peripherals.

4.8.1. Configure alternate boot mode selection pin

This section introduces how to customize the boot mode selection pins by programming the BOOTPIN_CONFIG position in the user-configurable DCS OTP. The position in the user DCS OTP is Z1_OTP_BOOTPIN_CONFIG. During debugging, EMU-BOOTPIN_CONFIG is simulation equivalence of Z1_OTP_BOOTPIN_CONFIG, which can be programmed for experiments using different boot modes without writing OTP. The device can be programmed as required to select pins using 0, 1, 2, or 3 boot modes.

Table 24 BOOTPIN_CONFIG Bit Field

Bit	Name	Description
7:0	Boot mode selection pin 0 (BMSP0)	Set to GPIO pins (up to 255) used during boot. 0x0 = GPIO0; 0x01 = GPIO1 and so on If all other BMSP are also set to 0xFF, 0xFF will be invalid and the default value BMSP0 will be selected. If any other BMSP is not set to 0xFF, setting BMSP to 0xFF will disable this specific BMSP.
15:8	Boot mode selection pin 1 (BMSP1)	Please refer to BMSP0 Description
23:16	Boot mode selection pin 2 (BMSP2)	Please refer to BMPS0 Description
31:24	Secret key	Write 0x5A into these 8 bits to inform the boot ROM code that the bits in this register are valid

Note: The following GPIO cannot be used as BMSP. If selected for a specific BMSP, the boot ROM will automatically select the default GPIO (the default value of BMSP2 is 0xFF, which will disable BMSP).

- GPIO 20 to 23
- GPIO 36
- GPIO 38
- GPIO 60 to 223

Table 25 Decoding of Independent Guidance Mode Selection Pins

BOOTPIN_CONFIG key	BMSP0	BMSP1	BMSP2	Implemented boot mode
!= 0x5A	No need for consideration	No need for consideration	No need for consideration	Boot defined by default BMSP (GPO24, GPO32)
= 0x5A	0xFF	0xFF	0xFF	Boot defined in the boot table of boot mode 3 (Disable all BMSP)
	Valid GPIO	0xFF	0xFF	Boot defined by the value of BMSP0 (Disable BMSP1 and BMSP2)
	0xFF	Valid GPIO	0xFF	Boot defined by the value of BMSP1 (Disable BMSP0 and BMSP2)
	0xFF	0xFF	Valid GPIO	Boot defined by the value of BMSP2 (Disable BMSP0 and BMSP1)
	Valid GPIO	Valid GPIO	0xFF	Boot defined by the values of BMSP0 and BMSP1 (Disable BMSP2)
	Valid GPIO	0xFF	Valid GPIO	Boot defined by the values of BMSP0 and BMSP2 (Disable BMSP1)
	0xFF	Valid GPIO	Valid GPIO	Boot defined by the values of BMSP1 and BMSP2 (Disable BMSP0)
	Valid GPIO	Valid GPIO	Valid GPIO	Boot defined by the values of BMSP0, BMPS1 and BMSP2

4.8.2. Configure alternate boot mode option

This section introduces how to configure the boot definition table BOOTDEF and related boot options for the device. 64-bit position is located in the user-configurable DCS OTP at the location of Z1_OTP_BOOTDEF_LOW and Z1_OTP_BOOTDEF_HIGH. During debugging, EMU_BOOTDEF_LOW and EMU_BOOTDEF_HIGH are simulation equivalence of Z1_OTP_BOOTDEF_LOW and Z1_OTP_BOOTDEF_HIGH, and can be programmed for experiments using different boot mode options without writing OTP. The custom range of the boot definition table depends on how many boot mode selection pins are being used.

Table 26 BOOTDEF Bit Field

BOOTDEF name	Byte position	Name	Description
BOOT_DEF0	7:0	BOOT_DEF0 mode and option	Set the boot mode and boot mode option. This may include changing the GPIO of specific boot peripherals or specifying different Flash entry points. Any unsupported boot mode will cause the device to reset. For valid BOOTDEF values, please refer to "GPIO Assignment".
BOOT_DEF1	15:8	BOOT_DEF1 mode and option	Please refer to BOOT_DEF0 Description.
BOOT_DEF2	23:16	BOOT_DEF2 mode and option	

BOOT_DEF3	31:24	BOOT_DEF3 mode and option	
BOOT_DEF4	39:32	BOOT_DEF4 mode and option	
BOOT_DEF5	47:40	BOOT_DEF5 mode and option	
BOOT_DEF6	55:48	BOOT_DEF6 mode and option	
BOOT_DEF7	63:56	BOOT_DEF7 mode and option	

4.8.3. GPIO Assignment

This section will introduce GPIO and the boot options for each boot mode set in BOOT_DEFx of Z1_OTP_BOOTDEF_LOW and Z1_OTP_BOOTDEF_HIGH. Please refer to "Configure Backup Boot Mode Selection Pins" to learn how to operate BOOT_DEFx. When selecting the boot mode option, please confirm that necessary pins are provided in the pin multiplexer option for the specific device package used.

Table 27 UART Boot Options

Option	The value of BOOTDEFx	UARTATX GPIO	UARTARX GPIO
0 (default value)	0x01	GPIO29	GPIO28
1	0x21	GPIO16	GPIO17
2	0x41	GPIO8	GPIO9
3	0x61	GPIO48	GPIO49
4	0x81	GPIO24	GPIO25

Note: Enable the pull-up resistors on UARTATX and UARTARX pins.

Table 28 CAN Boot Options

Option	The value of BOOTDEFx	CANTXA GPIO	CANRXA GPIO
0 (default value)	0x02	GPIO32	GPIO33
1	0x22	GPIO4	GPIO5
2	0x42	GPIO31	GPIO30
3	0x62	GPIO37	GPIO35

Note: Enable the pull-up resistors on CANTXA and CANARX pins.

Table 29 Flash Boot Options

Option	The value of BOOTDEFx	Flash entry point (address)	Flash memory bank, sector
0 (default value)	0x03	Flash - default option 1 (0x08000000)	Memory bank 0, Sector 0
1	0x23	Flash - option 2 (0x001000000)	Memory bank 0, Sector 14
2	0x43	Flash - option 3 (0x08020000)	Memory bank 1, Sector 0
3	0x63	Flash - option 4 (0x00120000)	Memory bank 1, Sector 14

Table 30 Wait Boot Options

Option	The value of BOOTDEFx	Watchdog status
0	0x04	Enabled
1	0x24	Disable

Table 31 SPI Boot Options

Option	The value of BOOTDEFx	SPIA_SIMO	SPIA_SOMI	SPIA_CLK	SPIA_STE
1	0x26	GPIO8	GPIO10	GPIO9	GPIO11
2	0x46	GPIO54	GPIO55	GPIO56	GPIO57
3	0x66	GPIO16	GPIO17	GPIO56	GPIO57
4	0x86	GPIO8	GPIO17	GPIO9	GPIO11

Note: Enable pull-up resistors on SPIA_SIMO, SPIA_SOMI, SPIA_CLK and SPIA_STE pins

Table 32 I2C Boot Options

Option	The value of BOOTDEFx	SDAA GPIO	SCLA GPIO
0	0x07	GPIO32	GPIO33
1	0x47	GPIO26	GPIO27
2	0x67	GPIO42	GPIO43

Note: Enable pull-up resistors on SDAA and SCLA pins.

Table 33 RAM Boot Options

Option	The value of BOOTDEFx	RAM entry point address
0	0x05	0x00000000（ITCM）
1	0x25	0x20100000（SRAM0）
2	0x45	0x20200000（SRAM1）
3	0x65	0x20300000（SRAM2）

Table 34 Secure Flash Boot Options

Option	The value of BOOTDEFx	Flash entry point (address)	Flash memory bank, sector
0	0x0A	0x00080000	Memory bank 0, Sector 0 (Busmatrix IF)
1	0x2A	0x00100000	Memory bank 0, Sector 0 (ITCM IF)
2	0x4A	0x08020000	Memory bank 1, Sector 0 (Busmatrix IF, DualBank Mode)
3	0x6A	0x00120000	Memory bank 1, Sector 0 (ITCM IF, DualBank Mode)

4.9. Dual-code Security Module

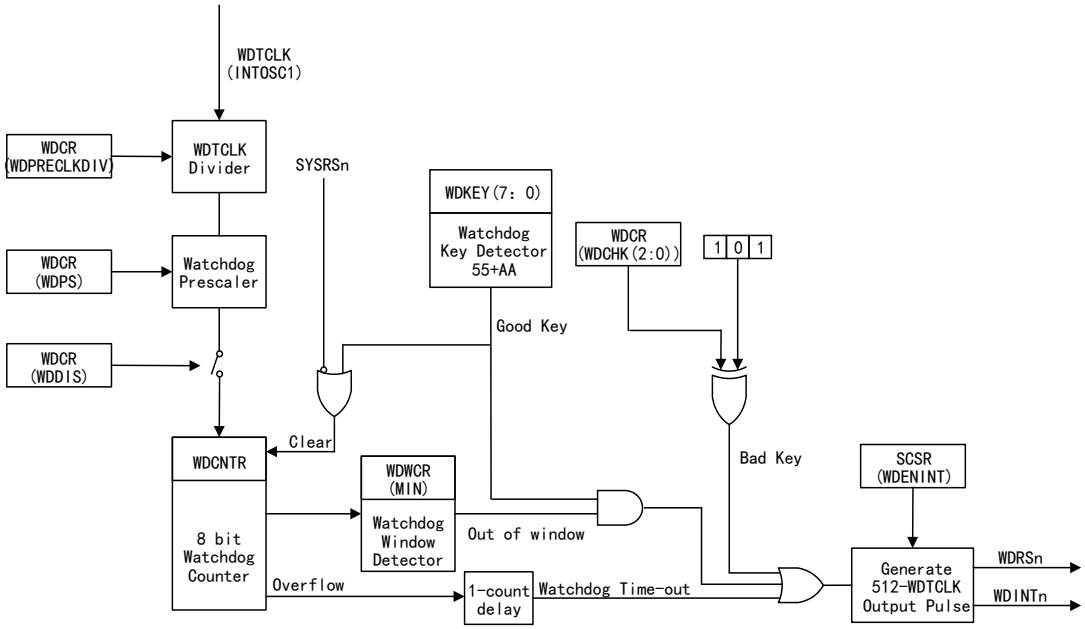
The dual-code security module (DCS) is designed to prevent unauthorized access and viewing of the on-chip security memories and other security resources. The term “secure” means preventing access to security memories and resources; the term “insecure” means allowing access. Please refer to *DCS User Manual* for more information about DCS functions.

4.10. Watchdog

The watchdog module provides an optional lower limit for the time between software resets of the counter, and this window countdown is disabled by default.

The watchdog generates a reset or interrupt. The watchdog uses an optional frequency divider for timing through an internal oscillator.

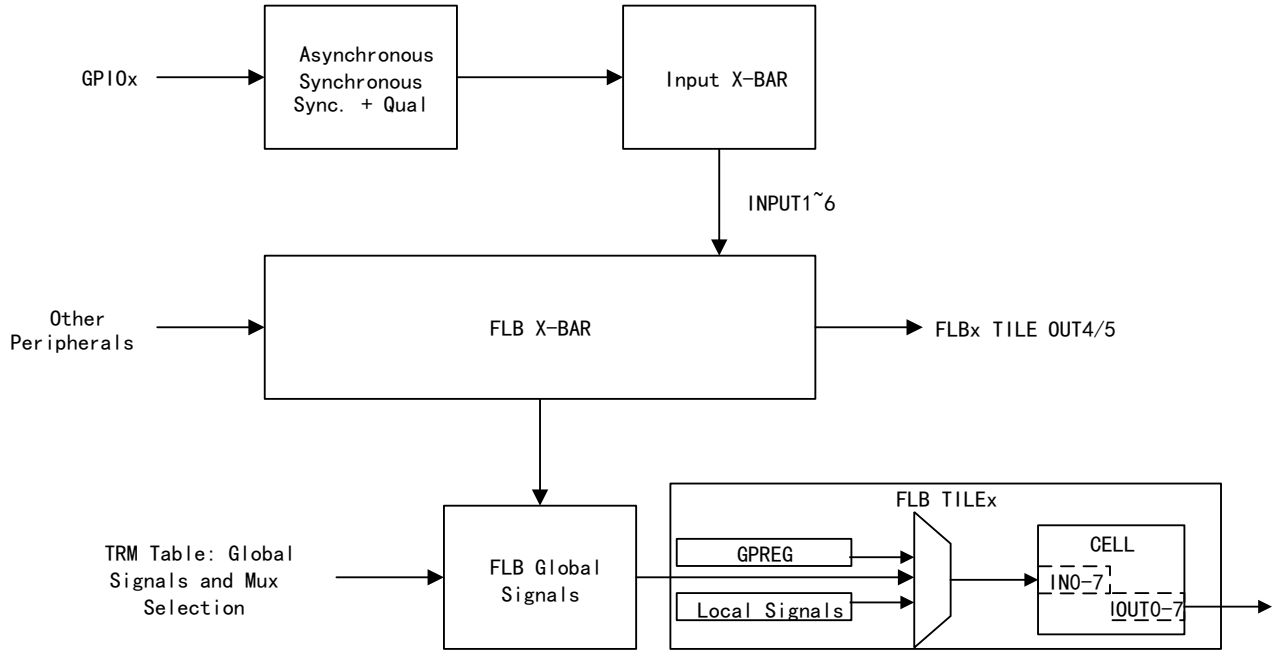
Figure 10 Watchdog Timer Structure Block Diagram



4.11. Flexible logic block (FLB)

Flexible logic block (FLB) is a set of configurable custom logic modules, and it can enhance existing peripheral interconnection through configuration, to provide high connectivity for on-chip control peripherals (PWM, CAP, and QEP).

Figure 11 TILE Connection from GPIO to FLB



4.12. Functional Safety

The functional safety compliant products are developed according to the hardware development process that conforms to IEC 61508 standard. This hardware has been evaluated and certified separately and meet the requirements of SIL2 system functions (see the certificates).

IEC61508 certification is in progress.

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

All data in this chapter is within the operating temperature range under natural ventilation conditions (unless otherwise specified). If the stress exceeds the absolute maximum tolerance values listed in the following table, permanent damage will be caused to the device. These are only stress tolerance values and do not indicate that the device can operate normally under these tolerance values or any other conditions beyond those described in this chapter. Long-term exposure to the absolute maximum tolerance may affect the reliability of the equipment. Unless otherwise specified, all voltage values are based on VSS. Long-term high-temperature storage or overdue use under maximum temperature conditions may shorten the total service life of the device. The continuous clamp current of each pin is ±2mA. Please do not operate the product continuously under these conditions, because VDDIO/VDDA voltage may rise internally and affect other electrical specifications.

5.1.1. Maximum temperature characteristics

Table 35 Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-65 ~ +150	℃
T_J	Maximum junction temperature	125/150	℃

5.1.2. Maximum rated voltage characteristics

Table 36Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{DD}	Supply voltage based on VSS	-0.3	1.3	V
V_{DDA}	Supply voltage based on VSSA	-0.3	4.125	
VDDIO	Supply voltage based on VSS	-0.3	4.125	
V_{IN}	Input voltage on 3.3V pins	-0.3	4.125	
V_O	Output voltage	-0.3	4.125	

5.1.3. Maximum rated current characteristics

Table 37 Maximum Rated Current Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
I_{IK} (V_{IN}< V_{SS} or V_{IN}> V_{DDIO})	Digital input (each pin)	-20	20	mA
$I_{IKANALOG}$ (V_{IN}< V_{SSA} or V_{IN}> V_{DDA})	Analog input (each pin)	-20	20	
$I_{IKTOTAL}$ (V_{IN}< V_{SS}/V_{SSA} or V_{IN}> V_{DDIO}/V_{DDA})	Total inputs	-20	20	
I_{OUT}	Digital output (each pin)	-20	20	

5.2. ESD Level - Commercial

Table 38 ESD Absolute Maximum Ratings

Symbol		Parameter	Condition	Pin	Range	Unit
100 pins						
V (ESD)	Electrostatic discharge	Human body model (HBM)	Conform to ANSI/ESDA/JEDEC JS-001 standard (1)		±4000	V
		Charging device model (CDM)	Conform to JEDEC, JESD22-C101 or ANSI/ESDA/JEDEC JS-002 (2)	All pins	±1000	
80 pins						
V (ESD)	Electrostatic discharge	Human body model (HBM)	Conform to ANSI/ESDA/JEDEC JS-001 standard (1)		±4000	V
		Charging device model (CDM)	Conform to JEDEC, JESD22-C101 or ANSI/ESDA/JEDEC JS-002 (2)	All pins	±1000	
64 pins						
V (ESD)	Electrostatic discharge	Human body model (HBM); conform to ANSI/ESDA/JEDEC JS-001 standard (1)			±4000	V
		Charging device model (CDM)	Conform to JEDEC, JESD22-C101 or ANSI/ESDA/JEDEC JS-002 (2)	All pins	±1000	
56 pins						
V (ESD)	Electrostatic discharge	Human body model (HBM)	Conform to ANSI/ESDA/JEDEC JS-001 standard (1)		±4000	V
		Charging device model (CDM)	Conform to JEDEC, JESD22-C101 or ANSI/ESDA/JEDEC JS-002 (2)		±1000	

Note:

(1) JEDEC document JEP155 states that 500V HBM can realize safe production under standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM can realize safe production under standard ESD control process.

5.3. Recommended Operating Conditions

Table 39 Recommended Operating Conditions

Symbol	Description	Minimum value	Typical value	Maximum value	Unit
V_{DDIO} and V_{DDA}	Enable internal BOR (1) for supply voltage of the device	$V_{BOR-VDDIO\ (MAX)} + V_{BOR-GB}$(2)	3.3	3.63	V
	Disable internal BOR for supply voltage of the	2.8	3.3	3.63	

Symbol	Description	Minimum value	Typical value	Maximum value	Unit
	device				
V_{DD}	Supply voltage of the device	1	1.1	1.2	V
VSS	Device grounding	0			V
VSSA	Analog ground	0			V
SR_{SUPPLY}	Power ramp rate (3)	-			-
$t_{VDDIO-RAMP}$	V_{DDIO} power ramp time (From 1V to $V_{BOR-VDDIO(MAX)}$)	10			ms
V_{BOR-GB}	VDDIO BOR guard band (4)	0.1			V
Junction temperature, T_J(5)		-40 ~ 125/150			°C
Ambient operating temperature, T_A		-40 ~ 125 / -40 ~ 105			°C

Note:

(1) Internal BOR is enabled by default.

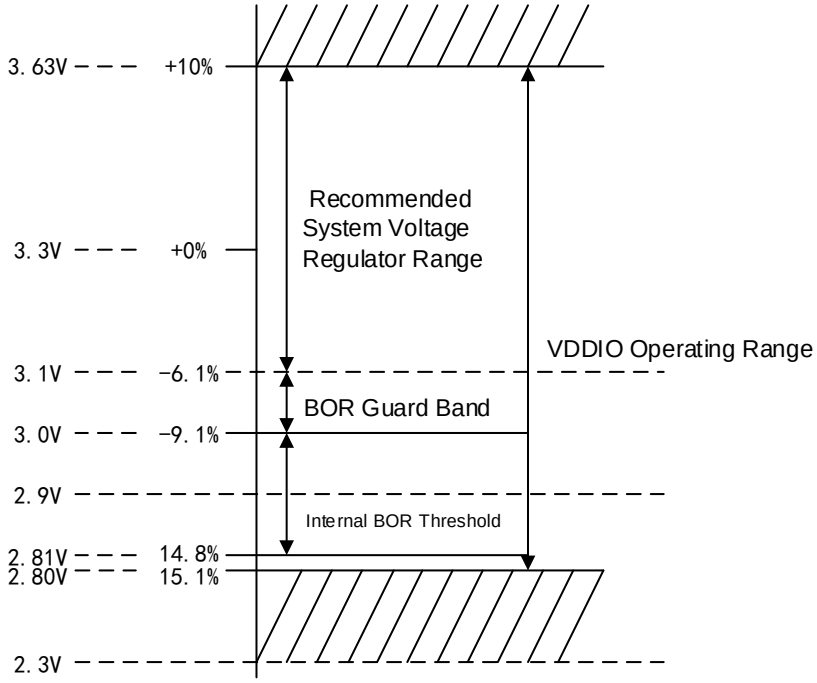
(2) VDDIO BOR voltage ($V_{BOR-VDDIO[MAX]}$) (see Electrical Characteristics) determines the lower voltage limit of the operating device. It is recommended that system designers should set an additional guard band (V_{BOR-GB}) in the budget, as shown in the following figure.

(3) Please refer to the table of operating conditions for power management module.

(4) It is recommended to use V_{BOR-GB} to avoid BOR reset caused by normal power supply noise or load transient events on 3.3V V_{DDIO} system voltage regulator. Good system voltage regulator design and decoupling capacitors (conforming to the system voltage regulator specifications) are crucial for preventing activation of BOR during normal operation of the device. The value of V_{BOR-GB} is a consideration in system-level design; the voltages listed here are typical values of many applications.

(5) Long-term operation at temperatures above T_J=105°C will shorten the service life of the device.

Figure 12 Supply Voltage



5.4. Power Consumption Summary

The current values listed in this section only represent values under the given test conditions and do not indicate the possible absolute maximum. In actual applications, the device current will vary depending on the application code and pin configuration.

5.4.1. System Current Consumption (VDD by External Power Supply)

The following measurements were taken within the ambient operating temperature (T_A) range under natural convection. The specific conditions are TYP: 25°C, 1.1V and MAX: 125°C, 1.1V.

Table 40 RUN Mode

Symbol	Parameter	Test conditions	MIN	TYP	MAX	MAX (125℃)	Unit
I_{DD}	V_{DD} current consumption in RUN	CPU0: Refer to the working mode test instructions CPU1: CoreMark FREQ: 250 MHz	84.0	85.5	86.5	168.7	mA
I_{DDIO}	V_{DDIO} current consumption in RUN		20.1	20.7	20.9	29.5	mA
I_{DDA}	V_{DDA} current consumption in RUN		10.5	10.7	10.8	10.8	mA

Table 41 IDLE Mode

Symbol	Parameter	Test conditions	MIN	TYP	MAX	MAX (125℃)	Unit
I_{DD}	V_{DD} current consumption in Idle	CPU in Idle mode Flash in Power down XCLKOUT is closed	50.4	51.6	52.5	139.6	mA
I_{DDIO}	V_{DDIO} current consumption in Idle		2.6	2.6	2.6	22.3	mA
I_{DDA}	V_{DDA} current consumption in Idle		0.23	0.24	0.27	0.27	mA

Table 42 STOP Mode

Symbol	Parameter	Test conditions	MIN	TYP	MAX	MAX (125℃)	Unit
I_{DD}	V_{DD} current consumption in STOP	CPU in STOP mode Flash in Power down XCLKOUT is closed	6.31	6.98	7.48	93.49	mA
I_{DDIO}	V_{DDIO} current consumption in STOP		2.18	2.21	2.22	17.11	mA
I_{DDA}	V_{DDA} current consumption in STOP		0.23	0.23	0.24	0.26	mA

5.4.2. System Current Consumption (VDD by Internal VREG Supply)

The following measurements were taken within the ambient operating temperature (T_A) range under natural convection. The specific conditions are TYP: 25°C, Vnom.

Table 43 RUN Mode

Symbol	Parameter	Test conditions	MIN	TYP	MAX	MAX (125℃)	Unit
I_{DDIO}	V_{DDIO} current consumption in RUN	CPU0: Refer to the working mode test instructions CPU1: CoreMark FREQ: 250 MHz	131.0	134.2	136.0	287.0	mA
I_{DDA}	V_{DDA} current consumption in RUN		10.0	10.2	10.4	12.0	mA

Table 44 IDLE Mode

Symbol	Parameter	Test conditions	MIN	TYP	MAX	MAX (125℃)	Unit
I_{DDIO}	V_{DDIO} current	CPU in Idle mode	63.0	64.8	66.0	197.0	mA

Symbol	Parameter	Test conditions	MIN	TYP	MAX	MAX (125℃)	Unit
	consumption in Idle	Flash in Power down XCLKOUT is closed					
I_{DDA}	V_{DDA} current consumption in Idle		0.23	0.23	0.23	0.26	mA

Table 45 STOP Mode

Symbol	Parameter	Test conditions	MIN	TYP	MAX	MAX (125℃)	Unit
I_{DDIO}	V_{DDIO} current consumption in STOP	CPU in STOP mode Flash in Power down XCLKOUT is closed	11.38	11.78	12.00	163.00	mA
I_{DDA}	V_{DDA} current consumption in STOP		0.23	0.23	0.24	0.26	mA

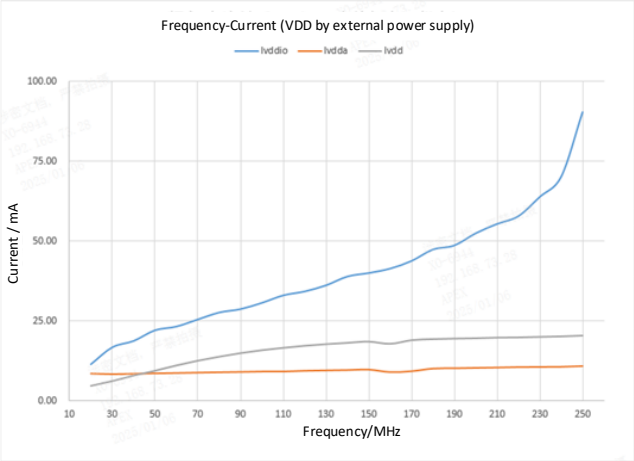
5.4.3. Work in Operating Mode

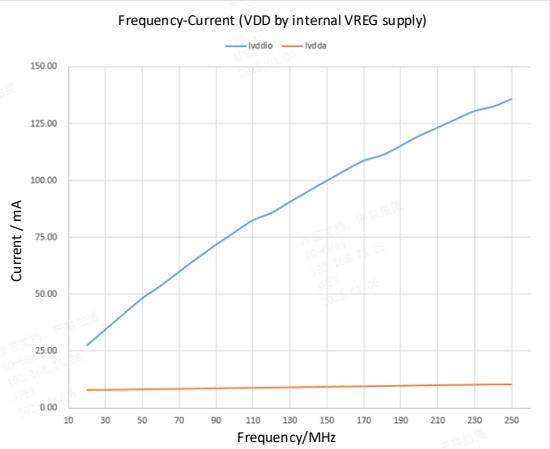
To achieve the indicated values, the following operations are performed in a loop in the test case. All other peripherals not listed below have their clocks disabled. The test conditions for CPU0's work mode are referenced in this chapter, and the conditions for CPU1's work mode follow the CoreMark program.

- Executing code from Flash
- Flash is read and remains active
- I/O pins do not drive any external components
- System frequency is 250 MHz, APB frequency is 125 MHz
- The following communication peripherals are used: SPIA, SPIB, UARTA, UARTB, CANA, CANB, LINA, PMBus, and QSPI
- PWM1 to PWM3 generate 5 MHz output on 6 pins
- PWM4 to PWM7 operate in HRPWM mode and generate 25 MHz output on 6 pins
- CPU timer is active
- CPU executes FIR16 calculations
- DMA performs continuous 32-bit transfers
- All ADCs perform continuous conversions
- All DACs change voltage at a loop frequency of about 11 kHz
- All COMPs generate a 100 kHz square wave
- SDF peripheral clock is enabled
- CAP1 to CAP7 operate in APWM mode with a switching frequency of 250 kHz
- All QEP watchdogs are enabled and perform counting
- The system watchdog is enabled and performs counting

5.4.4. Current Consumption Diagram

Below is a typical representation of the relationship between frequency and current consumption on this device. The operational tests in the "System Current Consumption (VDD by External Power Supply)" section are conducted over the full frequency range at V_NOM and room temperature. Actual results will vary depending on the system implementation and specific conditions.





5.4.5. Reducing Current Consumption

- To further lower the current consumption during idle periods in an application, you can enter either of the two low-power modes: Idle mode or Shutdown mode.
- If the code is executed from RAM, the Flash module can be powered down.
- Disable pull-up resistors on pins that are intended to function as outputs.
- Each peripheral has an individual clock enable bit (PCLKCRx). By turning off the clock for any peripheral not used in the application, you can reduce current consumption.

5.4.5.1. Peripheral Typical IDD

Table 46 Typical IDD of Peripheral

Peripheral(1)	**Typical IDD (mA)**
ADC(2)	0.8
CAN	1.0
FLB	1.0
COMP(2)	0.4
CPU Timer	0.3
DAC(2)	0.3
DMA	0.4
CAP1~ CAP5	0.1
CAP6~CAP7(3)	0.4
PWM	0.7
QEP	0.2
HRPWM	0.3
I2C	0.5
LIN	0.5
PMBUS	0.5
UART	0.9

Peripheral(1)	Typical IDD (mA)
SDF	0.9
SPI	0.2
QSPI	5.8
DCCOMP	0.4

Note:

(1) At reset, all peripherals are disabled. Use the PCLKCRx registers to enable each peripheral individually. For peripherals with multiple instances, the current is referenced on a per-module basis.

(2) This current represents the current drawn by the digital portion of each module.

(3) CAP6 and CAP7 can also be configured as HRCAP.

5.5. Electrical Characteristics

Table 47 Digital and Analog IO

Symbol	Parameter		Test conditions	Minimum value	Typical value	Maximum value	Unit
V_{OH}	High-level output voltage		I_{OH} = 1/2/4/6mA	V_{DDIO} * 0.8		V_{DDIO}	V
			I_{OH}=-100μA	V_{DDIO} – 0.2			
V_{OL}	Low-level output voltage		I_{OL}=1/2/4/6mA			0.4	V
			I_{OL} = 100μA			0.2	
I_{OH}	High-level output source current of all output pins		DS0/DS1=00@1mA DS0/DS1=01@2mA DS0/DS1=10@4mA DS0/DS1=11@6mA			-1 -2 -4 -6	mA
I_{OL}	Low-level output sinking current of all output pins		DS0/DS1=00@1mA DS0/DS1=01@2mA DS0/DS1=10@4mA DS0/DS1=11@6mA			1 2 4 6	mA
V_{IH}	High-level input voltage (3.3V)			2		V_{DDIO} + 0.3	V
VIL	Low-level input voltage (3.3V)			V_{SS}–0.3		0.8	V
$V_{HYSTERESIS}$	Input lag				200		mV
$I_{PULLDOWN}$	Input current	GPIO	V_{DDIO} = 3.3V V_{IN} = V_{DDIO}		160		μA
I_{PULLUP}	Input current	GPIO	V_{DDIO} = 3.3V V_{IN} = 0V		150		μA
		XRSN	V_{DDIO} = 3.3V V_{IN} = 0V		660		μA
I_{LEAK}	Pin leakage	Digital input	Pull-up, pull-down and			1	μA

Symbol	Parameter		Test conditions	Minimum value	Typical value	Maximum value	Unit
	current		output disabled $0V \le V_{IN} \le V_{DDIO}$				
		Analog pins (except VREFHIx and VREFLOx pins)	Analog driver disabled $0V \le V_{IN} \le V_{DDA}$			1	
		Analog pins (VREFHIx and VREFLOx pins)				0.1	
CI	Input capacitor	GPIO				10	pF
		XRSN				10	
		Analog pin	Analog pins are specified separately				

Table 48 VREG and BOR

Symbol	Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
$V_{POR-VDDIO}$	V_{DDIO} power-on reset voltage			2.3		V
$V_{BOR-VDDIO}$	V_{DDIO} undervoltage reset voltage		2.81	2.9	3.0	V
V_{VREG}	Internal voltage regulator output	Internal VREG enabled		1.1		V

5.6. Thermal Resistance Characteristics

Table 49 Thermal Resistance Characteristics of Package

Symbol	Parameter	°C/W (1)				Airflow (lfm) (2)			
		QFN56	LQFP64	LQFP80	LQFP100	QFN56	LQFP64	LQFP80	LQFP100
$R\Theta_{JC}$	Thermal resistivity to the shell surface	TBD	10.5	10.1	9.7	Not applicable	Not applicable	Not applicable	Not applicable
$R\Theta_{JB}$	Thermal resistivity to the circuit board	TBD	22.6	26.2	29.7	Not applicable	Not applicable	Not applicable	Not applicable
$R\Theta_{JA}$(high kPCB)	Thermal resistivity to the atmosphere	TBD	37.5	41.3	43.3	0	0	0	0

Symbol	Parameter	°C/W (1)				Airflow (lfm) (2)			
		QFN56	LQFP64	LQFP80	LQFP100	QFN56	LQFP64	LQFP80	LQFP100
$R\Theta_{JMA}$	Thermal resistivity to the flowing air	TBD	35.9	39.2	39.9	150	150	150	150
		TBD	33.2	37.1	38.2	250	250	250	250
		TBD	30.6	35.6	36.3	500	500	500	500

Note:

(1) The above values are based on the 2S2P system defined by JEDEC (excluding the values of Theta JC [$R\Theta_{JC}$] of 1S0P system defined based on JEDEC) and will change with the environment and application. For more information, please refer to the following EIA/JEDEC standards:

- JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements

(2) Fm=linear feet/minute

5.7. Precautions for Heat Dissipation Design

The current of I_{DD} and I_{DDIO} may vary according to the final application design and operating conditions. The system exceeding the recommended maximum power dissipation in the finished product may require extra heat dissipation enhancement measures. The ambient temperature (T_A) varies depending on the final application and product design. The key parameter affecting the reliability and functionality is the junction temperature T_J, rather than the ambient temperature. Therefore, be sure to maintain T_J within the specified limit. T_{case} should be measured to evaluate the operating junction temperature T_J. T_{case} is usually measured at the center of the top surface of the package.

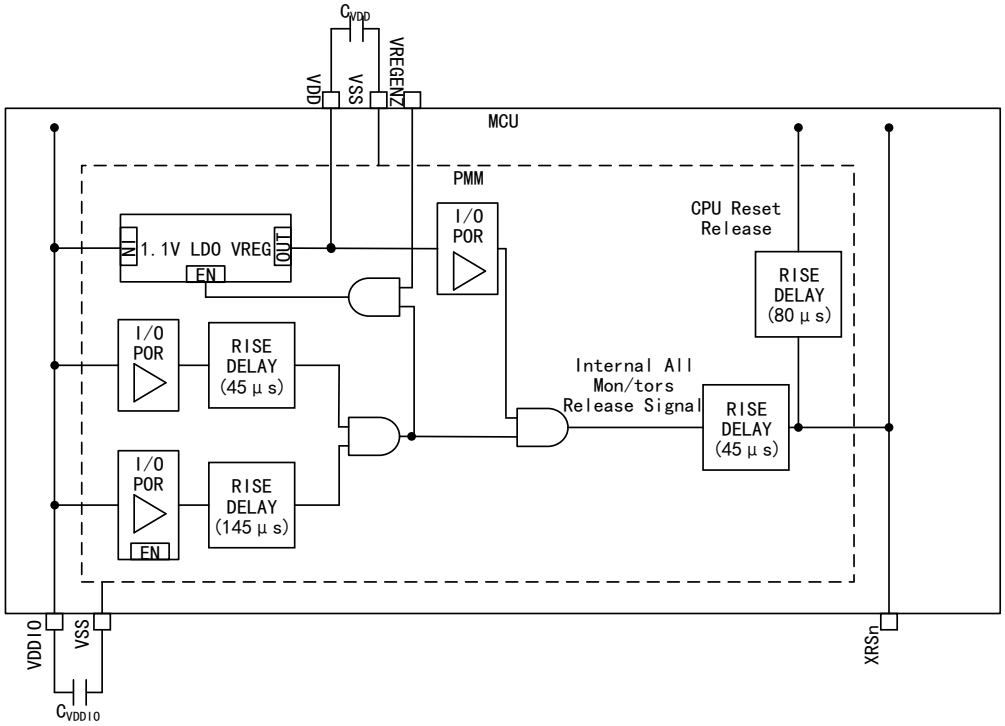
5.8. System

5.8.1. Power management unit (PMU)

PMM can handle all the power management functions required for running the device.

The block diagram of PMM is shown below. It can be seen that PMM contains multiple subcomponents, which will be introduced in subsequent chapters.

Figure 13 PMM Structure Block Diagram



5.8.1.1. Power rail monitor

PMM has a voltage monitor on the power rail. If the voltage exceeds the set threshold during power-on period, the XRSn signal will be released as a high level. If any voltage drops below the set threshold, these voltage monitors can also trip the XRSn signal to a low level. Various voltage monitors will be introduced in subsequent sections.

Note: If voltage monitors are not supported, and the device needs to monitor the supply voltage during application operation, it is recommended to use external monitors. The three voltage monitors, I/O POR, I/O BOR, and VDD POR, must release their respective outputs before the device starts running (i.e. XRSn becomes high). If any voltage monitor trips, XRSn will be driven to a low level. When any voltage monitor trips, I/O will maintain a high impedance.

I/O POR monitoring

Power on reset (I/O POR) is used to monitor the VDDIO power rail. In the power-on process of the chip, this is the first monitoring of releasing the trip on VDDIO.

I/O BOR monitoring

Undervoltage reset (I/O BOR) is also used to monitor the VDDIO power rail. During the power-on period, this is the second monitoring of releasing the trip on VDDIO. I/O BOR has stricter tolerance than I/O POR.

If the voltage drops below the recommended operating voltage, I/O BOR will be triggered to trip and the chip will be reset, but this function can be disabled by setting VMONCTL [BORLVMONDIS] to 1. I/O BOR can only be disabled after the chip is fully started. If I/O BOR is disabled, I/O POR will reset the chip when the voltage drops.

Note that the level of I/O POR tripping is much lower than the minimum recommended voltage of VDDIO, so it

should not be used for device monitoring.

Note that the level of I/O POR tripping is much lower than the minimum suggested voltage of VDDIO, so it should not be used for device monitoring.

VDD POR monitoring

VDD POR is used to monitor the VDD power rail. In the power-on process of the chip, if the voltage exceeds the trip level set by VDD, this monitoring circuit will release the trip .

Note: VDD POR is set at a level lower than the recommended minimum voltage for VDD. If it is necessary to monitor VDD in the application, external monitors should be used instead of relying on VDD POR monitoring.

5.8.1.2. Usage of external monitors

VDDIO monitoring: I/O BOR supports the application, so no external monitor is needed to monitor the I/O power rail.

VDD monitoring: VDD POR does not support the application. If the application requires VDD monitoring, an external monitor should be used to monitor the VDD power rail.

Note: External monitors can not be used together with the internal VREG. If the application requires detecting VDD, the VREGENZ pin package must be used to power the VDD externally.

5.8.1.3. Delay block

The delay block in the voltage monitor path is used to delay the release time between the voltage monitor and XRSn. When XRSn is released in external VREG mode, voltage stability can be ensured through delay. The delay block is only valid during power-on period of VDDIO and VDD. The delay block can help to achieve the minimum slew rate of the power rail specified in the Electrical Data and Timing of Power Management Module.

5.8.1.4. Internal 1.1V LDO voltage regulator (VREG)

The internal VREG is powered by the VDDIO power rail, and connecting the VREGENZ pin to a low level can generate the 1.1V voltage required to power the VDD pin. The internal VREG can be used, and VDD does not need to be powered externally. However, to ensure VREG stability and avoid transient, decoupling capacitors are still needed on the VDD pin. For detailed information, please refer to VDD Decoupling.

5.8.1.5. VREGENZ

The VREG disable pin can control the state of the internal VREG. To enable the internal VREG, the VREGENZ pin should be connected to a low level. For the application of external VREG, the VREGENZ pin should be connected to a high level to disable the internal VREG.

Note: The VREGENZ pin output function only exists on some package models. For detailed information, please refer to Pin Properties. The packages without VREGENZ do not support external VREG mode.

5.8.1.6. External components

5.8.1.6.1. Decoupling capacitor

VDDIO and VDD require decoupling capacitors to run properly. These requirements will be described in subsequent chapters.

VDDIO decoupling

A decoupling capacitor with the minimum capacitance value should be placed on VDDIO. Please refer to CVDDIO Parameters (located in the Electrical Data and Timing of Power Management Module). The decoupling capacitance value in actual use depends on the power supply driving the VDDIO. Any of the following configurations is acceptable:

- Configuration 1: Place a decoupling capacitor on each VDDIO pin according to the CVDDIO parameters.
- Configuration 2: Install a single decoupling capacitor equivalent to CVDDIO * VDDIO pin.

Note: It is crucial to place the decoupling capacitor (one or more) close to the device pins.

VDD decoupling

A decoupling capacitor with the minimum capacitance value should be placed on VDD. Please refer to C_{VDD} TOTAL Parameters (located in the Electrical Data and Timing of Power Management Module).

Any of the following configurations is acceptable:

- Configuration 1: Perform division operation on the CVDD TOTAL value on the VDD pin.
- Configuration 2: Install a decoupling capacitor with a capacitance value of CVDD TOTAL.

Note: It is crucial to place the decoupling capacitor (one or more) close to the device pins.

5.8.1.7. Power supply timing

5.8.1.7.1. Power pin linkage

It is recommended to connect all power pins of the power rail together internally. For example, all VDDIO pins are internally connected together, all VDD pins are internally connected together, and so on. No power pins should be suspended.

It is recommended that all 3.3V power rails should be connected together and be powered by a single power supply, including VDDIO and VDDA power rails.

In the internal VREG mode, connecting the VDD pins together is an optional operation, as long as there is a capacitor on each VDD pin. Please refer to "VDD Decoupling".

The analog module on the chip has a quite high PSRR (power supply rejection ratio). Therefore, in most cases, the noise on VDDA must exceed the recommended operating conditions of the power rail, which leads to performance degradation of the analog module. Therefore, the advantage of supplying VDDA alone is small. To improve the noise, the method of placing a π-type filter between VDDIO and VDDA can be adopted.

5.8.1.7.2. Power supply timing of signal pins

Before the chip is powered on, the voltage on any digital pin should not exceed VDDIO+0.3V, nor be lower than VSS-0.3V; the voltage on any analog pin (including VREFHI) should not exceed VDDA+0.3V, nor be lower than VSSA-0.3V.

To be brief, it is necessary to drive the signal pin after XRSn changes to a high level, provided that all 3.3V power rails are connected together. Even if VDDIO and VDDA are not connected together, the timing control is still required.

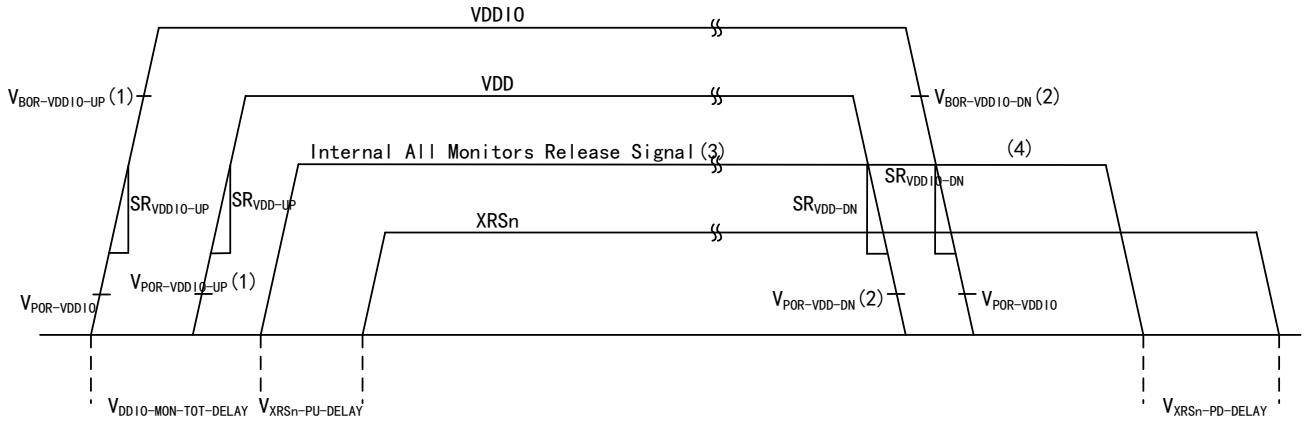
Note: If the above timing is violated, current may flow through unexpected parasitic paths in the chip, causing failures or damage to the chip.

5.8.1.7.3. Power supply sequence of power pins

External VREG/VDD mode sequence

The following figure shows the power supply timing control requirements for the external VREG mode. The values of all parameters can be found in the Electrical Data and Timing of Power Management Module.

Figure 14 External VREG Power-on Sequence



Note:

(1) The trip point is the trip point before the release of XRSn.

(2) The trip point is the trip point after the release of XRSn.

(3) During power-on period, the release signals of all monitor becomes high after all POR and BOR monitors are released.

(4) During power outage period, if any POR or BOR monitor trips, the release signal of all monitors will become low.

During power-on period:

- First, the 3.3V VDDIO power rail appears at the specified minimum slew rate
- Second, the 1.1V VDD power rail appears at the specified minimum slew rate
- The time difference between the appearance time of VDDIO power rail and VDD power rail is set
- After the specified time of VDDIO-MON-TOT-DELAY and VXRSN-PD-DELAY, XRSn will be released and the device will start the startup sequence. There is extra delay between the release of XRSn (i.e. becoming high) and the startup sequence.
- The I/O BOR monitor has different release points during power-on and power outage periods.

- During power-on period, both VDDIO and VDD power rails must be started before XRSn is released.

During power outage period:

- There is no requirement for which of VDDIO and VDD should be powered off first; but there is a specification of minimum slew rate
- The I/O BOR monitor has different release points during power-on and power outage periods
- Any POR or BOR monitor that trips during power outage will cause XRSn to become low after VXRSN-PD-DELAY

Note:

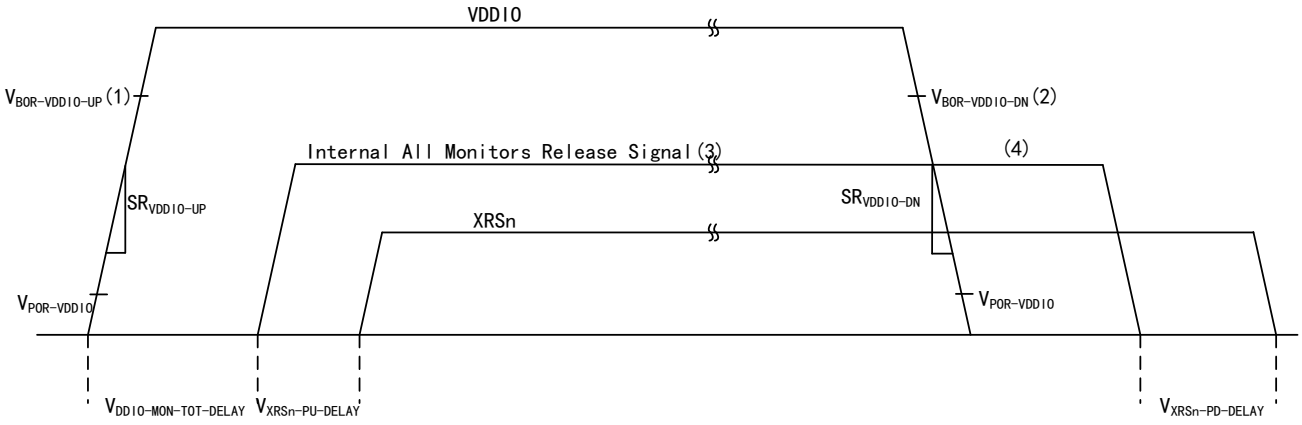
(1) The release signal of all monitors is an internal signal.

(2) If there is an external circuit (e.g. a monitor) that drives XRSn, the startup sequence will not be started before all internal and external sources release the XRSn pin.

Internal VREG/VDD mode sequence

The following figure shows the power supply timing control requirements for the internal VREG mode. The values of all parameters can be found in the Electrical Data and Timing of Power Management Module.

Figure 15 Internal VREG Power-on Sequence



Note:

(1) The trip point is the trip point before the release of XRSn.

(2) The trip point is the trip point after the release of XRSn.

(3) During power-on period, the release signals of all monitor becomes high after all POR and BOR monitors are released.

(4) During power outage period, if any POR or BOR monitor trips, the release signal of all monitors will become low.

During power-on period:

- The 3.3V VDDIO power rail appears at the specified minimum slew rate.

- The 1.1V VDD power rail appears at the specified minimum slew rate.
- The time difference between the appearance time of VDDIO power rail and VDD power rail is also set.
- After the specified time of VDDIO-MON-TOT-DELAY and VXRSN-PD-DELAY, XRSn will be released and the device will start the startup sequence. There is extra delay between the release of XRSn (i.e. becoming high) and the startup sequence.
- The I/O BOR monitor has different release points during power-on and power outage periods.
- During power-on period, both VDDIO and VDD power rails must be started before XRSn is released.

During power outage period:

- There is no requirement for which of VDDIO and VDD should be powered off first; but there is a specification of minimum slew rate.
- The I/O BOR monitor has different release points during power-on and power outage periods.
- I/O BOR tripping will cause XRSn to become low after $V_{XRSN-PD-DELAY}$, and power off the internal VREG.

Note:

(1) The release signal of all monitors is an internal signal.

(2) If there is an external circuit (e.g. a manager) that drives XRSn, the startup sequence will not be started before all internal and external sources release the XRSn pin.

Summary of power supply timing and impact of violations

The acceptable power-on sequence for the power rails is summarized as follows. The “power on” here indicates that the relevant power rail has reached the recommended minimum operating voltage. Unacceptable sequences can lead to a reliability problem and may result in damage. For simplicity, it is recommended to connect all 3.3V power rails together and operate according to the instructions in the power supply sequence of power pins.

Table 50 External VREG Sequence Summary

Situation	Power-on sequence of power rails			Acceptable
	VDDIO	V_{DDA}	V_{DD}	
A	1	2	3	Yes
B	1	3	2	Yes
C	2	1	3	-
D	2	3	1	-
E	3	2	1	-
F	3	1	2	-
G	1	1	2	Yes

H	2	2	1	-

Table 51 Internal VREG Sequence Summary

Situation	Power-on sequence of power rails		Acceptable
	VDDIO	V_{DDA}	
A	1	2	Yes
B	2	1	-
C	1	1	Yes

Note: The analog module on the device should only be powered after VDDA reaches the recommended minimum operating voltage.

Supply voltage slew rate

- VDDIO has requirements for the minimum slew rate.

When the minimum slew rate requirement is not met, XRSn may switch multiple times before VDDIO exceeds the I/O BOR region. In general, switching on XRSn has no adverse effects on the chip, and XRSn will boot only when it is stable at a high level. But if the XRSn of this chip is used to control the reset signals of other IC, the slew rate requirement must be met to prevent such switching of XRSn.

- VDD has a minimum slew rate requirement in external VREG mode.

When the minimum voltage swing requirement is not met, the chip may release a reset and boot before VDD reaches the minimum operating voltage, so that the chip may be unable to operate normally.

If the minimum voltage swing requirement cannot be met, a monitor must be used on VDD to keep XRSn at a low level until VDD exceeds the minimum operating voltage threshold, so as to ensure that the chip can operate normally.

5.8.1.8. Electrical data and timing of power management module

Table 52 Operating Conditions for Power Management Module

Symbol	Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
General						
C_{VDDIO}	Large-capacity capacitors on VDDIO	Based on external power IC requirements (1)		0.1		μF
C_{VDDIO_DCAP}	Decoupling capacitor on each VDDIO pin			0.1		μF
C_{VDDA}	Capacitor on VDDA pin			2.2		μF
C_{VDD}	Large-capacity capacitors on VDD	Suitable for LDO-only working mode (2)	12	20	27	μF
C_{VDD_DCAP}	Decoupling capacitor on each VDD pin	Suitable for LDO-only working mode (2)	0.1		6.75	μF
SR_{VDDIO_UP}(4)	Power ramp-up rate of		8		100	mV/μs

Symbol	Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
	3.3V power rail (VDDIO)					
$SR_{VDDIO-DN}$ (4)	Power ramp-down rate of 3.3V power rail (VDDIO)		20		100	mV/μs
External VREG						
C_{VDD} total (3) (5)	Total VDD capacitance (7)		10			μF
SR_{VDD-UP} (4)	Power ramp-up rate of 1.1V power rail (VDD)		3.5		100	mV/μs
SR_{VDD-DN} (4)	Power ramp-down rate of 1.1V power rail (VDD)		10		100	mV/μs
V_{DDIO} - V_{DD} delay (6)	Slope delay between VDDIO and VDD		0		Unlimited	μs

Note:

(1) The large-capacity capacitor on this power supply should be based on the requirements of the power IC.

(2) For detailed information, please refer to "Internal 1.1V LDO Voltage Regulator (VREG)".

(3) The exact value of the decoupling capacitor depends on the voltage regulation solution to the system that supplies power to these pins.

(4) Please refer to "Supply Voltage Slew Rate". If the power ramp rate is higher than the maximum value, on-chip ESD protection will be triggered.

(5) For possible configuration of total decoupling capacitors, please refer to "Power Management Module (PMM)".

(6) The delay between the 3.3V power rail ramp-up and the 1.1V power rail ramp-up. For the allowed power ramp sequence, please refer to the table of "VREG Sequence Summary".

(7) The maximum capacitor tolerance should be 20%.

Table 53 Characteristics of Power Management Module

Symbol	Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
V_{VREG}	Internal voltage regulator output		1.07	1.1	1.14	V
$V_{VREG-PU}$	Power-on time of internal voltage regulator		80		340	μs
$V_{VREG-INRUSH}$ (5)	Surge current of internal voltage regulator		354		662	mA
$VPOR_{-VDDIO}$	VDDIO power-on reset voltage	Before and after XRSn release		2.3		V
$V_{BOR-VDDIO-UP}$ (1)	VDDIO undervoltage reset voltage during ramp-up	Before XRSn release		2.9		V

Symbol	Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
$V_{BOR-VDDIO-DN}$(1)	VDDIO undervoltage reset voltage during ramp-down	After XRSn release	2.81		3.00	V
$V_{POR-VDD-UP}$（2）	VDD power-on reset voltage during ramp-up	Before XRSn release		0.72		V
$V_{POR-VDD-DN}$(2)	VDD power-on reset voltage during ramp-down	After XRSn release		0.72		V
$V_{XRSn-PU-DELAY}$(3)	XRSn release delay after power ramp-up during power-on period	This is final delay		248		μs
$V_{XRSn-PD-DELAY}$(4)	XRSn trip delay after power ramp-down during power outage period			26		μs
$V_{DDIO-MON-TOT-DELAY}$	Total delay in VDDIO monitor (POR, BOR) path			318		μs
$V_{XRSn-MON-RELEASE-DELAY}$	XRSn release delay after VDD POR	The power supply is within the working range		248		μs
	XRSn release delay after VDDIO BOR			586		μs
	XRSn release delay after VDDIO POR			509		μs

Note:

(1) Please refer to the diagram of "Supply Voltage".

(2) $V_{POR-VDD}$ is not supported, as it is set to trip at a level lower than the recommended operating conditions. If VDD needs to be monitored, an external monitor is required.

(3) The power supply is considered to fully ramp up after crossing the recommended minimum operating conditions of corresponding power rail. Before the delay takes effect, all POR and BOR monitors need to be released. The RC network delay will be added to this delay.

(4) In case of power outage, any tripped POR or BOR monitor will immediately cause XRSn to trip. This delay is the time between any POR, BOR monitor trip and XRSn becoming low. The delay is a variable, which depends on the power ramp-down rate. The RC network delay will be added to this delay.

(5) This is the transient current drawn on the VDDIO power rail when the internal VREG is conducting. Therefore, when VREG is conducting, there may be some voltage drop on the VDDIO power rail, which may cause VREG to gradually ramp up. This will have no adverse effects on the device, but if necessary, the effect can be reduced by using sufficient decoupling capacitors on VDDIO or selecting the LDO that can provide this transient current.

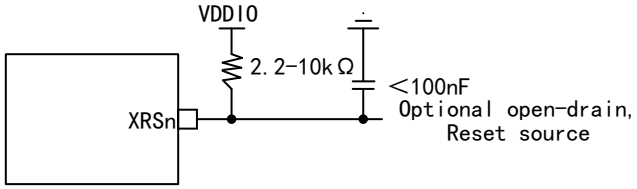
5.8.2. Reset timing

XRSn is used as the reset pin for the chip. When powered on, the POR circuit built into the chip will pull down

the XRSn pin, the watchdog (WWDT, NMIWDT) reset will also pull down the pin, and the external circuit may drive the pin to make the device reset take effect.

It is recommended to place a resistor with a resistance of 2.2kΩ to 10kΩ between XRSn and VDDIO; and place a capacitor with a capacitance of less than 100nF between XRSn and VSS for noise filtering. When the watchdog reset takes effect, these values enable the watchdog to correctly drive the XRSn pin to VOL within 512 OSCCLK cycles. Figure 7-12 shows the recommended reset circuit.

Figure 16 Reset Circuit



5.8.2.1. Reset source

Table 54Reset Signals

Reset source	CPU core reset (CPU, FPU, VCU)	Peripheral reset	JTAG/Debugging logic reset	I/O	XRSn output
POR	Yes	Yes	Yes	High-impedance state	Yes
XRSn pin	Yes	Yes	No	High-impedance state	-
WDRS	Yes	Yes	No	High-impedance state	Yes
NMIWDRS	Yes	Yes	No	High-impedance state	Yes
SYSRS (debugger reset)	Yes	Yes	No	High-impedance state	No
SCCRESET	Yes	Yes	No	High-impedance state	No

Note:

(1) Resets initiated from these sources must be considered for the parameter th (boot mode).

(2) Some reset sources are driven internally by the device. Some of these sources will drive XRSn to a low level to disable any other devices that drive the boot pins. SCCRESET and debugger reset sources will not drive XRSn; therefore, the pins used for the boot mode should not be actively driven by other devices in the system. Boot configuration allows changing the boot pins in OTP.

5.8.2.2. Reset electrical data and timing

Table 55 Reset (XRSn) Timing Requirements

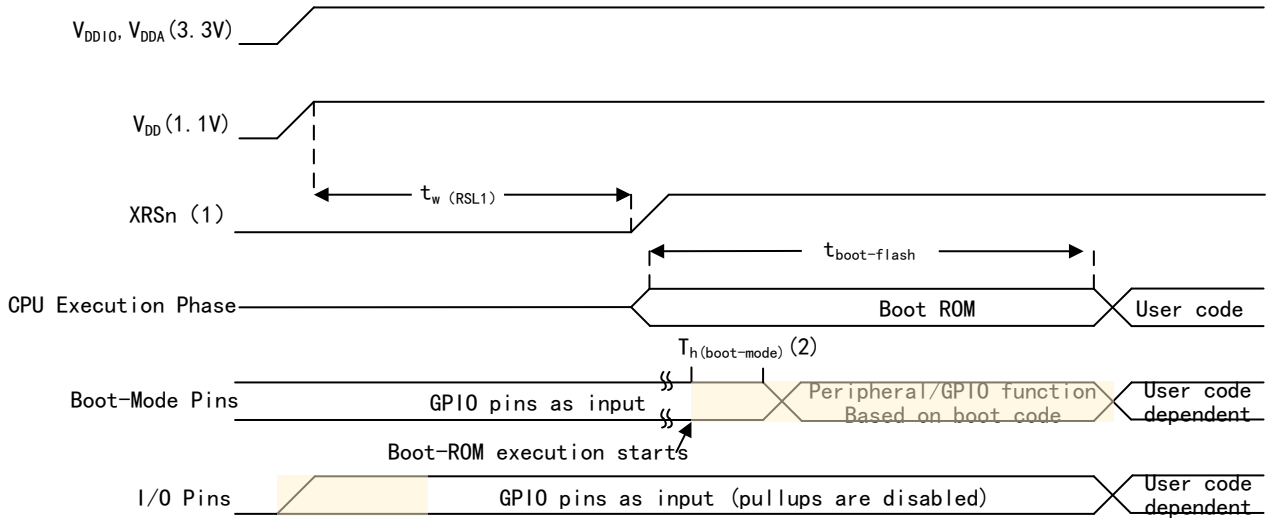
Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
t_h (boot mode)	Holding time of boot mode pin		1.5		ms

$t_{w\ (RSL2)}$	Pulse duration; XRSn is at a low level during hot reset	All situations	74		μs
		Low-power mode used in the application, and SYSCLKDIV>16	3.2*(SYSCLKDIV/16)		

Table 56 Characteristics of Reset (XRSn) Switch

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
tw (RSL1)	Pulse duration	XRSn is driven to a low level by the device after the power supply is stabilized		241		us
$t_{w(WDRS)}$	Pulse duration	Reset pulse generated by watchdog		810tc （OSCCLK）		Cycle
$t_{boot-flash}$	Execution time of Boot ROM before the first instruction fetch in Flash				900	μs

Figure 17 Power-on Reset

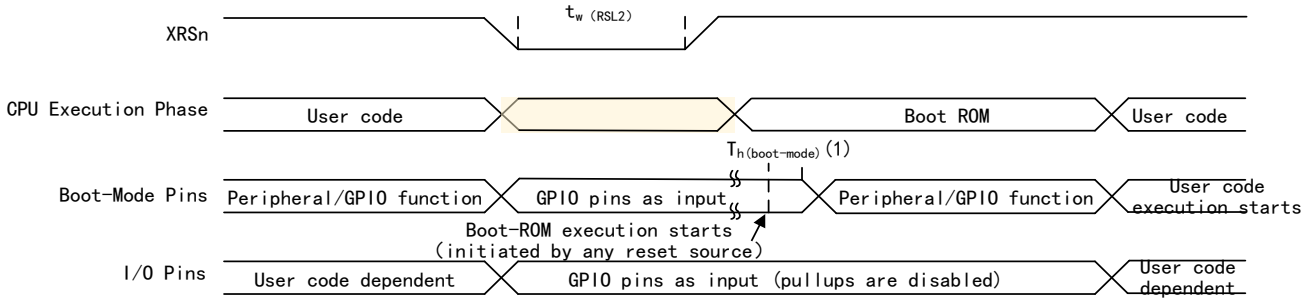


Note: SYSCLK will be based on the user environment, and PLL can be enabled or disabled.

(1) XRSn pin can be driven externally by a monitor or an external pull-up resistor; please refer to "Pin Properties". The on-chip POR logic will keep this pin low until the power supply falls within the valid range.

(2) After reset from any source (see Reset Sources), the boot ROM code will sample the boot mode pins. Based on the status of boot mode pin, the boot codes are branched to the destination memory or boot code function. If the boot ROM code is executed after the power-on conditions (in the debugging program environment), the execution time of the boot code is based on the current SYSCLK speed.

Figure 18 Hot Reset



Note: SYSCLK will be based on the user environment, and PLL can be enabled or disabled.

(1) After reset from any source (see Reset Sources), the boot ROM code will sample the boot mode pins. Based on the status of boot mode pin, the boot codes are branched to the destination memory or boot code function. If the boot ROM code is executed after the power-on conditions (in the debugging program environment), the execution time of the boot code is based on the current SYSCLK speed.

5.8.3. Clock specifications

5.8.3.1. Clock source

Table 57 Possible Reference Clock Sources

Clock source	The module has timed	Comment
INTOSC1	Can be used to provide clocks for the following modules: Watchdog module Main PLL CPU timer 2	Internal oscillator 1 10MHz internal oscillator for zero pin overhead
INTOSC2 (1)	Can be used to provide clocks for the following modules: Main PLL CPU timer 2	Internal oscillator 2 10MHz internal oscillator for zero pin overhead
X1 (XTAL)	Can be used to provide clocks for the following modules: Main PLL CPU timer 2	The external crystal or resonator connected between pins X1 and X2, or a single-ended clock connected to pin X1.

Note:

(1) When reset, the internal oscillator 2 (INTOSC2) serves as the default clock source of the system PLL (OSCCLK).

Figure 19 Clock Source

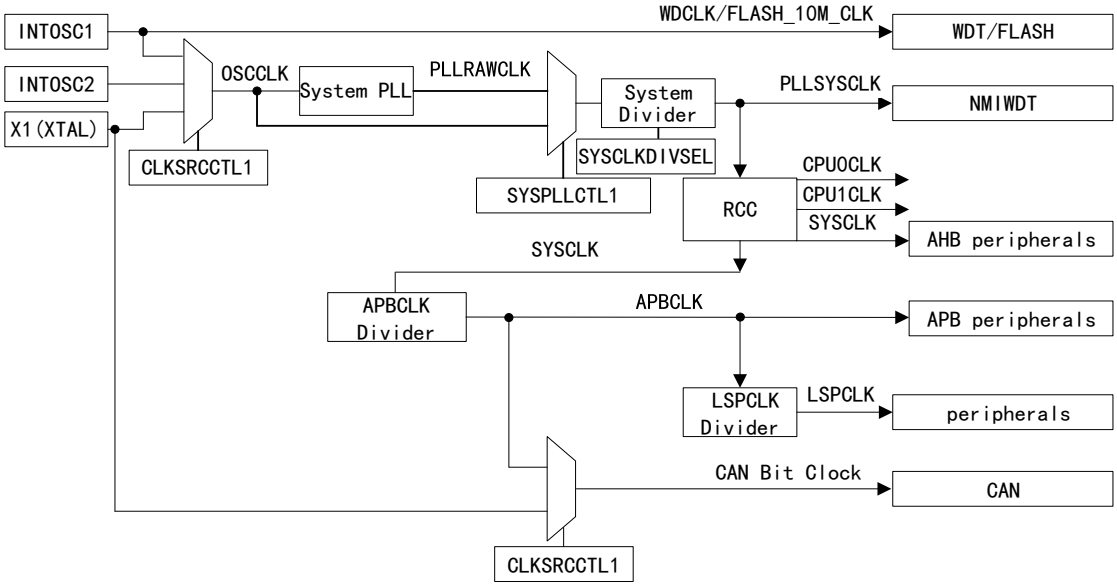
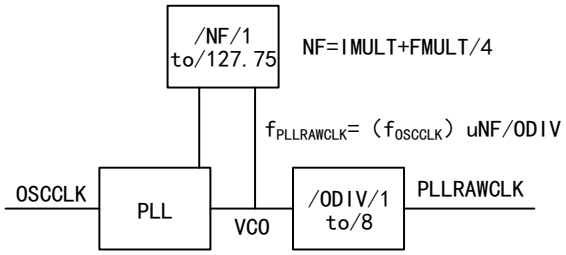


Figure 20 System PLL



5.8.3.2. Clock frequency, requirements, and characteristics

This section provides the frequency and timing requirements and PLL locking time of input clock, internal clock frequency, output clock frequency and switch characteristics.

5.8.3.2.1. Frequency and timing requirements, and PLL lock time of input clock

Table 58 Input Clock Frequency

Symbol	Parameter	Minimum value	Maximum value	Unit
$f_{(XTAL)}$	Frequency, X1/X2, from external crystal or resonator	10	20	MHz
$f_{(X1)}$	Frequency, X1, from external oscillator	2	20	MHz

Table 59 Characteristics of XTAL Oscillator

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
X1 VIL	Valid low-level input voltage	-0.3		0.3 * VDDIO	V
X1 VIH	Valid high-level input voltage	0.7 * VDDIO		VDDIO + 0.3	V

Table 60 X1 Timing Requirements

Symbol	Parameter	Minimum value	Maximum value	Unit
$t_{f\ (X1)}$	Fall time, X1		9	ns
$t_{r\ (X1)}$	Rise time, X1		12	ns
$t_{w\ (X1L)}$	Pulse duration, percentage of X1 low level in $t_{c\ (X1)}$	45%	55%	
$t_{w\ (X1H)}$	Pulse duration, percentage of X1 high level in $t_{c\ (X1)}$	45%	55%	

Table 61 PLL Locking Time

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
$t_{(PLL)}$	Locking time, main PLL		232μs+ 1024 * $t_{c\ (OSCCLK)}$		μs

5.8.3.2.2. Internal clock frequency

Table 62 Internal Clock Frequency

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
$f_{(SYSCLK)}$	Frequency, device (system) clock	2		250	MHz
$t_{c(SYSCLK)}$	Cycle, device (system) clock	4		500	ns
$f_{(VCO)}$	Frequency, PLL VCO (before the output divider)	120		600	MHz
$f_{(PLLRAWCLK)}$	Frequency, system PLL output (before SYSCLK divider)	15		250	MHz
$f_{(PLL)}$	Frequency, PLLSYSCLK	2		250	MHz
$f_{(APBCLK)}$	Frequency, APBCLK	2		125	MHz
$t_{c(APBCLK)}$	Cycle, APBCLK	8		500	ns
$f_{(LSP)}$	Frequency, LSPCLK	2		125	MHz
$t_{c(LSPCLK)}$	Cycle, LSPCLK	8		500	ns
$f_{(OSCCLK)}$	Frequency, OSCCLK (INTOSC1, INTOSC2, XTAL or X1)	Refer to respective clocks			MHz
$f_{(HRPWM)}$	Frequency, HRPWMCLK	60		125	MHz

5.8.3.2.3. Output clock frequency and switch characteristics

Table 63 XCLKOUT Switch Characteristics

Symbol	Parameter (1)	Minimum value	Maximum value	Unit
$t_{f(XCO)}$	Fall time, XCLKOUT		5	ns
$t_{r\ (XCO)}$	Rise time, XCLKOUT		5	ns
$t_{w(XCOL)}$	Pulse duration, XCLKOUT low level	H–2 (2)	H+2 (2)	ns
$t_{w(XCOH)}$	Pulse duration, XCLKOUT high level	H–2 (2)	H+2 (2)	ns
$f_{(XCO)}$	Frequency, XCLKOUT		50	MHz

Note:

(1) Assuming these parameters have a load of 40pF.

(2) H = 0.5$t_{c\,(XCO)}$

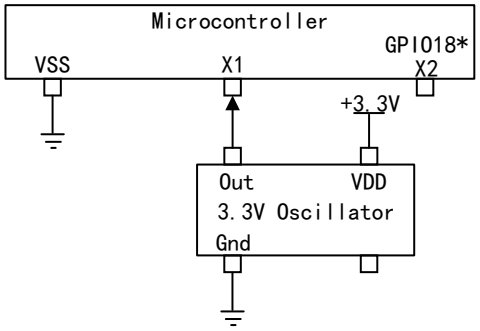
5.8.3.3. Input clock

GPO18* and its multiplexer options can only be used when the system is timed by INTOSC and X1 has an external pull-down resistor.

In addition to the internal 0-pin oscillator, it also supports three types of external clock sources:

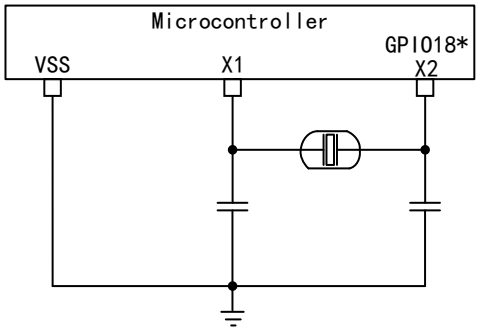
(1) Single-ended 3.3V external clock. The clock signal should be connected to X1 and XTALCR.SE bit should be set to 1.

Figure 21 Single-ended 3.3V External Clock



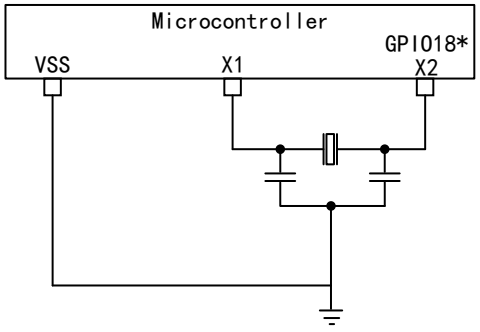
(2) External crystal The crystal should be connected between X1 and X2, with its load capacitor connected to VSS.

Figure 22 External Crystal



(3) External resonator. The resonator should be connected between X1 and X2, and its ground terminal should be connected to VSS.

Figure 23 External Resonator



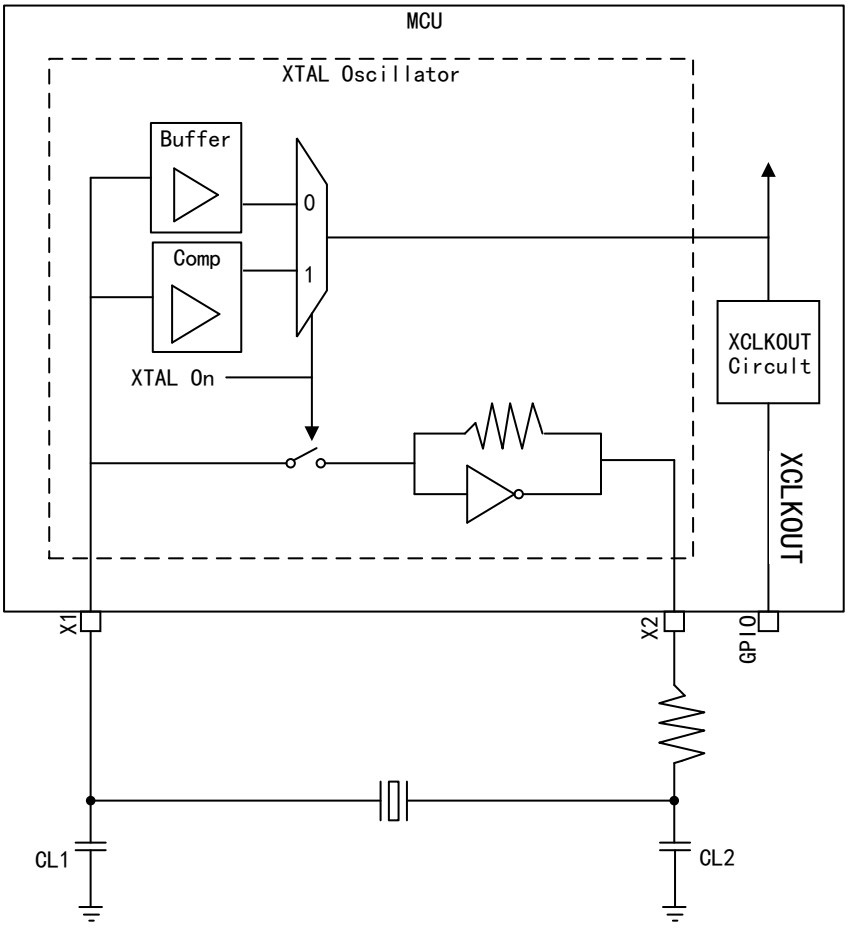
5.8.3.4. Crystal (XTAL) oscillator

The crystal oscillator in this device is an embedded electrical oscillator, which can generate the system clock required by the device when it is paired with the compatible quartz or ceramic crystal oscillators.

5.8.3.4.1. Electronic oscillator

When the electronic oscillator in this device is paired with a compatible crystal oscillator, an oscillation circuit will be formed. The oscillation circuit oscillates at the fundamental frequency of the crystal. On this device, the oscillator is designed to operate in parallel resonant mode due to the bridging capacitor (C0) and the required load capacitor (CL). The following figure shows the components of the electronic oscillator and oscillation circuit.

Figure 24 Structure Block Diagram of Electronic Oscillator



Operation Modes

The electric oscillator in this device has two operating modes: crystal mode and single-ended mode.

(1) Operating mode of crystal

In the operating mode of crystal, the quartz crystal with a load capacitor must be connected to X1 and X2.

When [XTAL On] =1, this operating mode can be enabled by setting XTALCR.OSCOFF = 0 and XTALCR.SE= 0. The feedback loop has an internal bias resistor. If an external bias resistor is added, a resistance in parallel

with the internal bias resistor will be generated, which will move the operating bias point and may cause waveform clipping, duty cycle exceeding specifications, and reduction of effective negative resistance. Therefore, external bias resistors should not be used

In this operating mode, the result clock on X1 is transmitted to the remaining modules of the chip through the comparator. The clock on X1 needs to meet the VIH and VIL of the comparator. For the VIH and VIL requirements of the comparator, please refer to XTAL Oscillator Characteristic Table.

(2) Single-ended operating mode

In single-ended operating mode, a clock signal is connected to X1 while X2 is suspended. The quartz crystal should not be used in this mode.

When [XTAL On] =0, this operating mode can be enabled by setting XTALCR[OSCOFF]= 1 and XTALCR[SE]= 1.

In this operating mode, the clock on X1 is transmitted to the rest of the chip through a buffer. For the input requirements of the buffer, please refer to X1 Input Level Characteristic Table when an external clock source (non-crystal) is used.

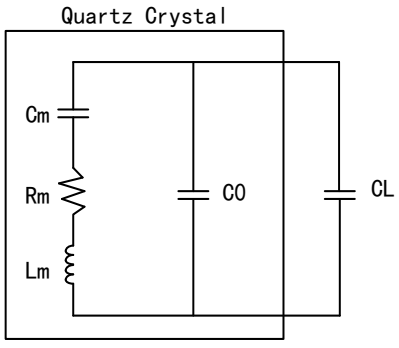
XTAL output on XCLKOUT

By configuring CLKSRCCTL3.XCLKOUTSEL and XCLKOUTDIVSEL.XCLKOUTDIV registers, the output of the oscillator fed into other part of the chip can be led out to XCLKOUT for observation. To view the list of GPIO of XCLKOUT output, please refer to the table of "GPIO Multiplexing Pin".

5.8.3.4.2. Quartz crystals

The quartz crystals can be electrically represented by LCR (inductive - capacitive - resistive) circuits. However, unlike LCR circuits, the crystals have a very high Q value due to their low dynamic resistance, and their damping is also very low.

Figure 25 Electrical Representation of Crystals



Note:

(1) Cm (dynamic capacitance): Represents the elasticity of the crystal.

(2) Rm (dynamic resistance): Represents resistance loss within the crystal. This is not equivalent resistance of a crystal, but it can be approximately calculated based on the values of other crystal components.

(3) Lm (dynamic inductance): Represents the vibrational mass of the crystal.

(4) C0 (parallel Capacitor): A capacitor formed by two crystalline electrodes and stray package capacity.

(5) CL (load capacitance): This is the effective capacitance seen by the crystal at its electrodes. It is located outside the crystal and used for crystal frequency pulling. The frequency ppm indicated in the crystal data table is usually associated with the parameter CL.

For the definition of CL values, please consult corresponding crystal oscillator manufacturer so as to use correct values in calculation.

CL1 and CL2 are connected in series; therefore, to find the equivalent total capacitance of the crystal, the capacitance series formula must be applied. It is recommended to add the stray PCB capacitance to this value.

Note: Both the electric oscillator and the crystal require a load capacitor, so the selected capacitance value must meet the requirements of both the electric oscillator and the crystal oscillator.

5.8.3.4.3. GPIO operating mode

On this device, X2 can serve as GPO18, depending on the operating mode of XTAL.

5.8.3.4.4. Normal operation

ESR - effective series resistance

Equivalent series resistance is the resistive load provided by the crystal to the electronic oscillator during resonance. The higher the ESR, the lower the quality of the capacitor, and the less likely the crystal is to start or maintain oscillation. The relationship between ESR and crystal components is shown below.

$$ESR = Rm * \left(1 + \frac{C0}{CL}\right)^2$$

Note: ESR is different from dynamic resistance of the crystal, but if the effective load capacitance is much higher than the shunt capacitance, it can be approximately calculated according to it.

Rneg (negative resistance)

Negative resistance is the impedance presented by the electric oscillator to the crystal. This is the energy that the electric oscillator must provide to the crystal in order to overcome the losses generated during oscillation. Rneg describes a circuit that provides energy instead of consuming it, and can also be seen as the overall gain of the circuit.

To ensure that the crystal can start under all conditions, it is recommended that Rneg should be greater than 3 to 5 times the ESR.

The negative resistance change curve shows the difference between the negative resistance of the device and the crystal element. From the figure, it can be seen that the crystal parallel capacitance (C0) and effective load capacitance (CL) have a huge impact on the negative resistance of the electric oscillator. For the minimum and maximum values that should be noted in the design, please refer to the table of " Requirements for Equivalent Series Resistance (ESR) of Crystal Oscillators" .

Startup time

The crystal ESR and damping resistance (Rd) will greatly affect the startup time. The higher these two values, the longer it takes for the crystal to start. If the startup time is long, it indicates that the crystal and elements are not matched correctly.

For the startup time, please refer to the Specifications of Crystal Oscillators. The actual startup time also depends on the crystals and external elements involved.

DL (drive level)

Drive level refers to the amount of power provided by the electronic oscillator and dissipated by the crystal.

If the actual drive level of the electronic oscillator exceeds the maximum drive level specification of the crystal, a damping resistor (Rd) should be installed to limit the current and reduce the power dissipation of the crystal. The damping resistor Rd can reduce the circuit gain. Therefore, the actual values to be used should be evaluated to ensure that all other conditions for startup and sustained oscillation are met.

5.8.3.4.5. How to choose crystals

Please refer to the Specifications of Crystal Oscillators:

(1) Choose a crystal frequency (e.g. 20MHz).

(2) Confirm that the ESR of the crystal is less than or equal to 50Ω, and conforms to the 20MHz specification.

(3) Confirm that the load capacitance of the crystal manufacturer should be between 6pF and 12pF, and conforms to the 20MHz specification.
- CL1 and CL2 are connected in series. Therefore, if CL1=CL2, the effective load capacitance CL=[CL1]/2.
- On this basis, and in combination with the parasitic effect of the circuit board, CL=[CL1]/2+stray capacitance can be obtained.

(4) Confirm that the maximum drive level of the crystal is greater than or equal to 1mW. If this requirement is not met, a damping resistor Rd can be used. For other key points to be considered when using Rd, please refer to DL - Drive Level.

5.8.3.4.6. Test

For detailed parameters of crystal resonators, please consult corresponding manufacturers.

Measurement of some parameter is listed below:

As the crystal circuit is very sensitive to capacitance, it is recommended not to connect the oscilloscope probe to X1 and X2. If an oscilloscope probe must be used to monitor X1/X2, an active probe with a capacitance less than 1pF shall be used.

- Frequency

(1) Lead out XTAL on XCLKOUT

(2) Measure this frequency as the crystal frequency

- Negative resistance

(1) Lead out XTAL on XCLKOUT

(2) Place a potentiometer connected in series with the crystal between the load capacitors

(3) Increase the resistance of the potentiometer until the clock on XCLKOUT stops

(4) This resistance plus the actual ESR of the crystal is negative resistance of the electric oscillator

- Startup time

(1) Disable XTAL

(2) Lead out XTAL on XCLKOUT

(3) Enable XTAL and measure the time required for the clock on XCLKOUT to remain within the 45% and 55% duty cycle range

5.8.3.4.7. Common problems and prompts for debugging

(1) The crystal cannot start

- Browse how to select the crystal part and ensure there are no violations.

(2) The crystal takes a long time to start

- If the damping resistor Rd is installed, it will be too high.
- If no damping resistor is installed, the crystal ESR will be too high or the total circuit gain will be too low due to high load capacitance.

5.8.3.4.8. Specifications of Crystal Oscillators

Table 64 Crystal Oscillator Parameters

Symbol	Parameter	Minimum value	Maximum value	Unit
CL1, CL2	Load capacitance	12	24	pF
C0	Parallel capacitance of crystal oscillator		7	pF

Table 65 Equivalent Series Resistance (ESR) Requirements for Crystal Oscillators

Crystal frequency (MHz)	Maximum ESR (Ω) (CL1 = CL2 = 12pF)	Maximum ESR (Ω) (CL1 = CL2 = 24pF)
10	55	110
12	50	95
14	50	90
16	45	75
18	45	65
20	45	50

Note:

(1) The parallel capacitance (C0) of the crystal oscillator should be less than or equal to 7pF.

(2) ESR=Negative resistance/3

Table 66 Electrical Characteristics of Crystal Oscillators

Parameter		Test conditions	Minimum value	Typical value	Maximum value	Unit
Startup time (1)	f = 10MHz	Maximum value of ESR =110Ω CL1 = CL2 = 24pF C0 = 7pF		8		ms
	f = 20 MHz	Maximum value of ESR =50Ω CL1 = CL2 = 24pF C0 = 7pF		8		ms
Drive level of crystal oscillator (DL)					1	mW

Note:

(1) The startup time depends on the crystal and oscillating circuit components.

5.8.3.5. Internal oscillators

In order to reduce the production cost of circuit boards and shorten the application development time, the devices all include two independent internal oscillators, called INTOSC1 and INTOSC2. By default, both oscillators are enabled when powered on. INTOSC2 is set as the system reference clock (OSCCLK) source, and INTOSC1 is set as the backup clock source. INTOSC1 can also be manually configured as the system reference clock (OSCCLK). The electrical characteristics of the internal oscillators are provided in the following table to determine whether this module meets the timing requirements of the application.

Table 67 INTOSC Characteristics

Symbol	Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
f_{INTOSC}	Frequency, INTOSC1 and INTOSC2		9.7	10	10.3	MHz
$f_{INTOSC-STABILITY}$	Frequency stability at room temperature	30°C, nominal VDD		±0.1%		
	Frequency stability on VDD	30°C		±0.2%		
	Frequency stability		-3%		3%	
$t_{INT0SC-ST}$	Start and settling time			20		μs

5.8.3.6. PLL

Table 68 PLL Power Consumption and Leakage

Mode	**Condition**	**Minimum value**	**Typical value**	**Maximum value**	**Unit**
Normal	0.9v, 1v, 1.1v full process angle -40° C, 30° C, 125° C	1.2	2	3	mA
Shutdown			5	15	μA

Table 69 PLL Characteristics

Parameter	Description	Minimum value	Typical value	Maximum value	Unit
f_{ref}	Reference frequency	2	10	20	MHz
N_{PLL}	Feedback frequency dividing ratio	1		127.75	
S_{fra}	Decimal step		0.25		
N_{PLL_OUT}	Output frequency dividing ratio	1		8	
T_{PLL}	Locking time	25.5μs+1024*tc (oscclk)			μs
F_{VCO}	VCO frequency	120		600	MHz
f_{out}	PLL output frequency	15		300	MHz

5.8.4. Flash parameters

Table 70 Minimum Flash Wait Cycles (FRDCNTL[RWAIT]) Required at Different System Frequencies

System Frequencies	RWAIT(1)
0＜f≤36MHz	0
36＜f≤72MHz	1
72＜f≤108MHz	2
108＜f≤144MHz	3
144＜f≤180MHz	4
180＜f≤216MHz	5
216＜f≤250MHz	6

Note:

(1) To increase the system frequency, first configure RWAIT to the target frequency range and then increase the system frequency. To reduce the system frequency, first configure the system frequency to lower the clock, and then configure RWAIT to the target frequency range.

Table 71 Flash Parameters

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
tpgh	Programming waiting time	20			ns
tprog	Programming time			15	μs
tme	Mass erasing time	20		100	ms
durability	Program/Erase cycle (Endurance)		10K		Cycles
Read the cycle time				25	ns
$t_{retention}$ data retention duration (T_J=125℃)		10			Year

Note: The recommended operating conditions are TA= -40℃~125℃, VDD= 1.0V~1.2V, VDDIO= 2.8V~3.63V, VSS=0V, CLOAD= 0.01pf

5.8.5. Simulation

The G32R501 series provides a wide range of debugging, tracing, and testing features. They adopt the standard Arm® CoreSight™ module configuration and connect via a daisy-chain standard TAP controller. The debugging and tracing functions are integrated in the Arm® Cortex®-M52. In addition to standard JTAG debugging, the debugging system also supports Serial Wire Debug (SWD) and trace capabilities. For details on debugging and tracing features, refer to the《*Arm China Processor Technical Reference Manual*》.

The JTAG (IEEE 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture) port has four dedicated pins: TMS, TDI, TDO, and TCK. cJTAG (IEEE Standard 1149.7-2009 Reduced Pin and Enhanced Functionality Test Access Port and Boundary Scan Architecture) port is a compact JTAG interface that only requires two pins (TMS and TCK), which can serve other device function of multiplexing into traditional GPO35 (TDI) and GPO37 (TDO) pins.

Generally, when the distance between the MCU target and the JTAG connector is less than 15cm and there are no other devices on the JTAG chain, no buffer is required on the JTAG signal. Otherwise, every signal should be buffered. Besides, for most JTAG debugging probe operations at 10MHz, no series resistor is needed on the JTAG signal. However, if high simulation speed (around 35MHz) is required, a 22Ω resistor should be connected in series to each JTAG signal.

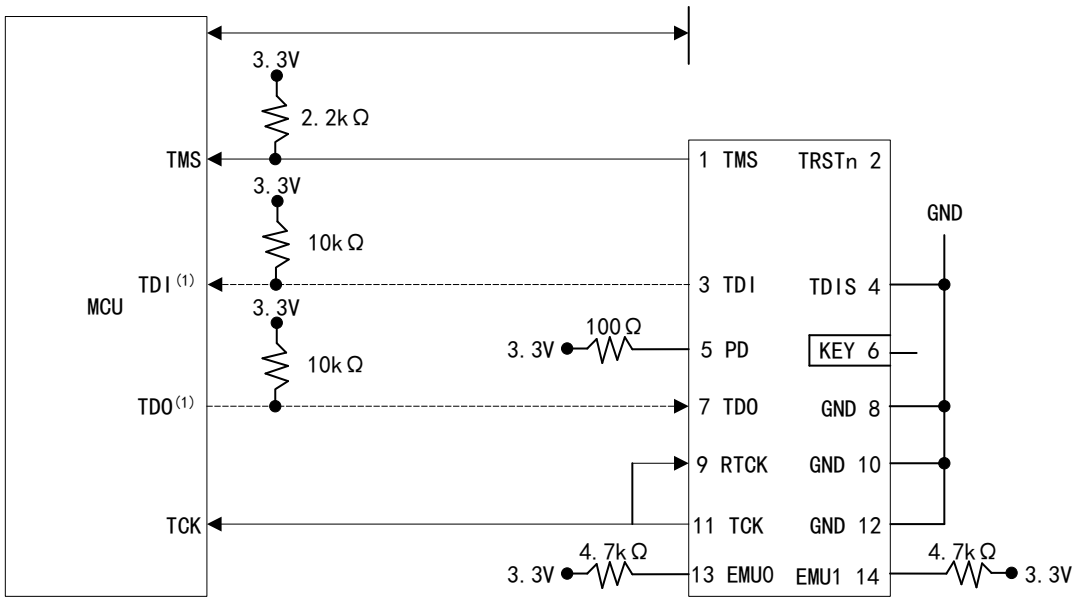
The PD (power detection) terminal of the JTAG debugging probe should be connected to 3.3V power supply of the circuit board. The GND terminal of the connector should be connected to the circuit board ground. TDIS (cable disconnect sensor) should also be connected to the circuit board ground. The JTAG clock should be looped back from the TCK output terminal of the connector to the RTCK input terminal of the connector (in order to detect the clock continuity through JTAG debugging probe). This MCU does not support EMU0 and EMU1 signals on 14-pin and 20-pin simulation connectors. These signals should always be pulled up at the simulation connector through a pair of on-board pull-up resistors ranging from 2.2kΩ to 4.7kΩ (depending on the driving strength of the debugger port). Usually a resistance of 2.2kΩ is used.

Terminal reset of the connector is open-drain output of the JTAG debugging probe connector, and through the JTAG debugging probe command, the circuit board components are reset (only available through the 20-pin connectors).

JTAG test data input (TDI) is the default multiplexer selection for pins. By default, the internal pull-up resistor is disabled. If this pin serves as JTAG TDI, an internal pull-up resistor should be enabled or an external pull-up resistor should be added on the circuit board to avoid suspension of input. In cJTAG option, this pin can serve as GPIO.

JTAG test data output (TDO) is the default multiplexer selection for pins. By default, the internal pull-up resistor is disabled. When there is no JTAG activity, the TDO function will be in a three-state condition, causing this pin to be suspended. An internal pull-up resistor should be enabled or an external pull-up resistor should be added on the circuit board to avoid suspension of input. In cJTAG option, this pin can serve as GPIO.

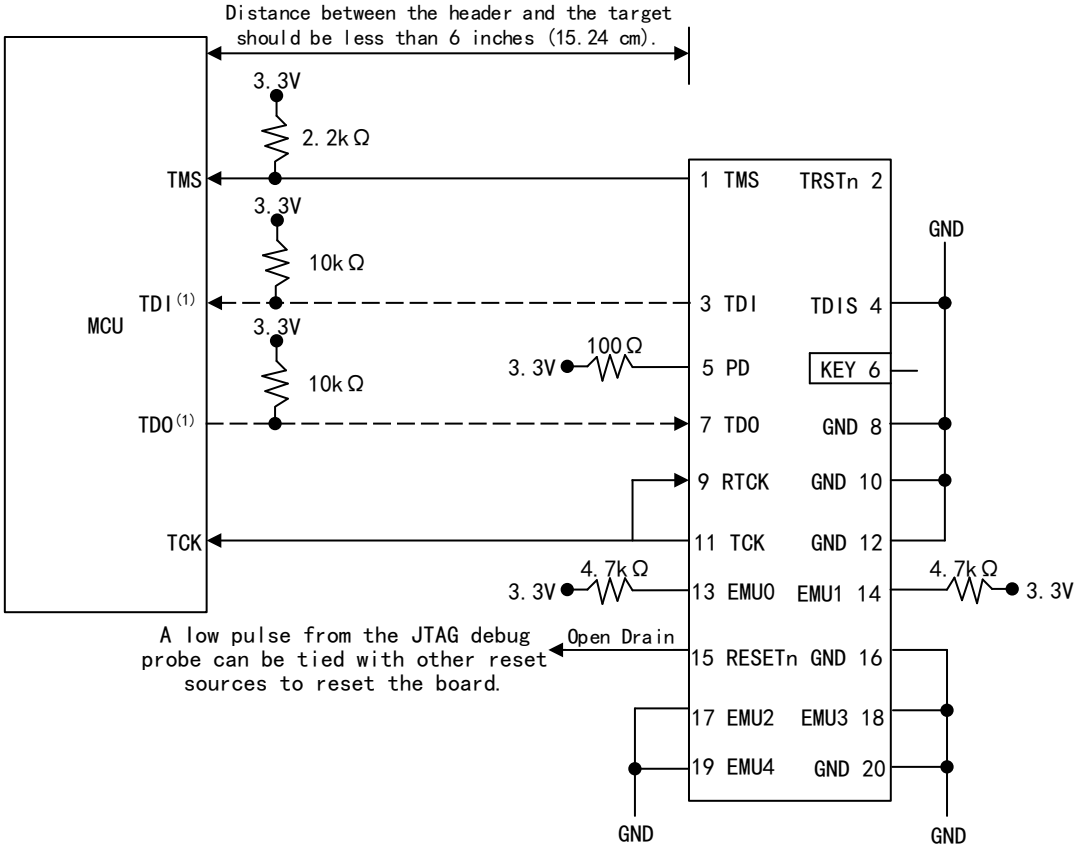
Figure 26 Connect to 14-pin JTAG Connector



Note:

(1) cJTAG option does not require connection of TDI and TDO, and these pins can be used as GPIO.

Figure 27 Connect to 20-pin JTAG Connector



Note:

(1) cJTAG option does not require connection of TDI and TDO, and these pins can be used as GPIO.

5.8.5.1. Electrical data and timing of JTAG

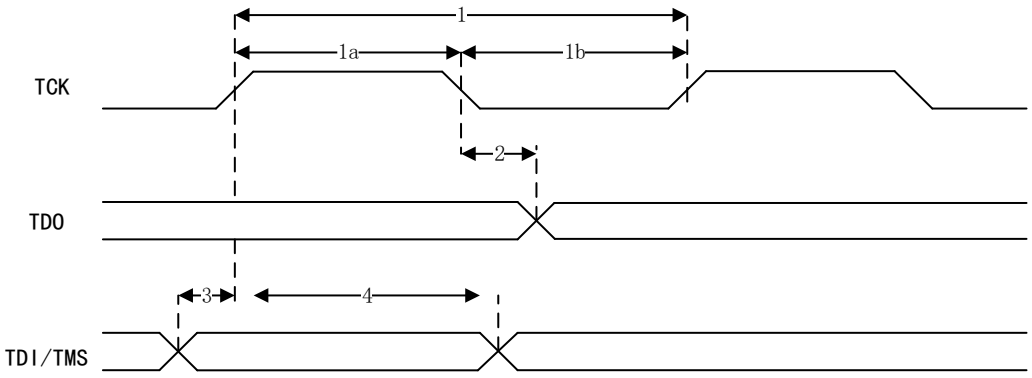
Table 72 JTAG Timing Requirements

No.	Symbol	Parameter	Minimum value	Maximum value	Unit
1	$t_{c(TCK)}$	Cycle time, TCK	66.66		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high level (40% of tc)	26.66		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low level (40% of tc)	26.66		ns
3	$t_{su(TDI-TCKH)}$	Input set time from TDI becoming valid to high level of TCK	13		ns
	$t_{su(TMS-TCKH)}$	Input set time from TMS becoming valid to high level of TCK	13		
4	$t_{h(TCKH-TDI)}$	Input holding time from high level of TCK to TDI becoming valid	7		ns
	$t_{h(TCKH-TMS)}$	Input holding time from high level of TCK to TMS becoming valid	7		

Table 73 JTAG Switch Characteristics

No.	Symbol	Parameter	Minimum value	Maximum value	Unit
2	$t_{d(TCKL-TDO)}$	Delay time from low level of TCK to TDO becoming valid	6	25	ns

Figure 28 JTAG Timing



5.8.5.2. Electrical data and timing of cJTAG

Table 74 cJTAG Timing Requirements

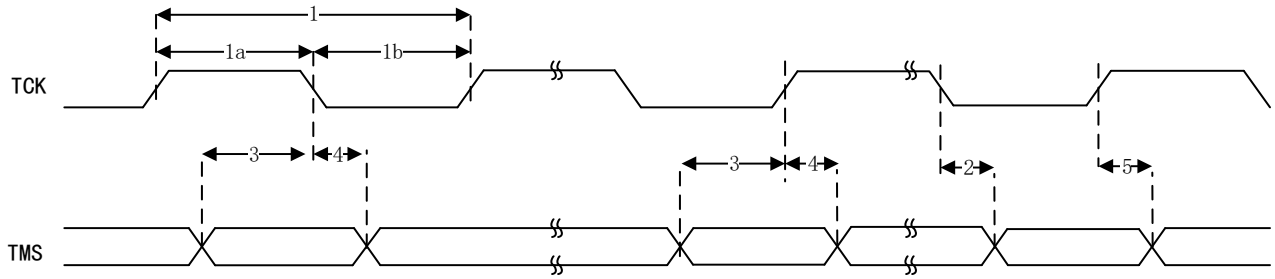
No.	Symbol	Parameter	Minimum value	Maximum value	Unit
1	$t_{c(TCK)}$	Cycle time, TCK	100		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high level (40% of tc)	40		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low level (40% of tc)	40		ns
3	$t_{su(TMS-TCKH)}$	Input set time from TMS becoming valid to	15		ns

		high level of TCK			
	$t_{su(TMS-TCKL)}$	Input set time, from TMS becoming valid to low level of TCK	15		ns
4	$t_{h(TCKH-TMS)}$	Input holding time from high level of CK to TMS becoming valid	2		ns
	$t_{h(TCKL-TMS)}$	Input holding time, from low level of TCK to TMS becoming valid	2		ns

Table 75 cJTAG Switch Characteristics

No.	Symbol	Parameter	Minimum value	Maximum value	Unit
2	$t_{d(TCKL-TMS)}$	Delay time, the time from low level of TCK to TMS becoming valid	6	20	ns
5	$t_{dis(TCKH-TMS)}$	Delay time, the time from high level of TCK to disabling of TMS		20	ns

Figure 29 cJTAG Timing Diagram



5.8.6. Electrical data and timing of GPIO

Peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. When resetting, the GPIO pin is configured as input. For specific inputs, users can also choose the number of input qualification periods to filter out unnecessary noise interference.

The GPIO module includes the output X-BAR, which allows routing various internal signals to the GPIO in GPIO multiplexer position and is represented as OUTPUTXBARx. The GPIO module also includes the input X-BAR, which is used to route signals from any GPIO input to different IP blocks, for example ADC, CAP, PWM, and external interrupts.

5.8.6.1. GPIO output timing

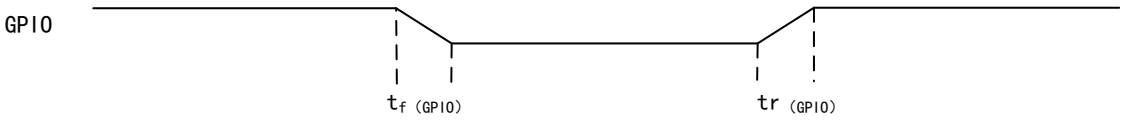
Table 76 General-purpose Output Switch Characteristics

Symbol	Parameter	Minimum value	Maximum value	Unit
$t_{r(GPIO)}$	Rise time, GPIO switches from a low level to a high level		8 (1)	ns
$t_{f(GPIO)}$	Fall time, GPIO switches from a high level to a low level		8 (1)	ns
f_{GPIO}	Switching frequency		60	MHz

Note:

(1) The rise time and fall time vary with the load. These values are based on the assumption of a load of 40pF.

Figure 30 General-purpose Output Timing



5.8.6.2. GPIO input timing

Table 77 General-purpose Input Timing Requirements

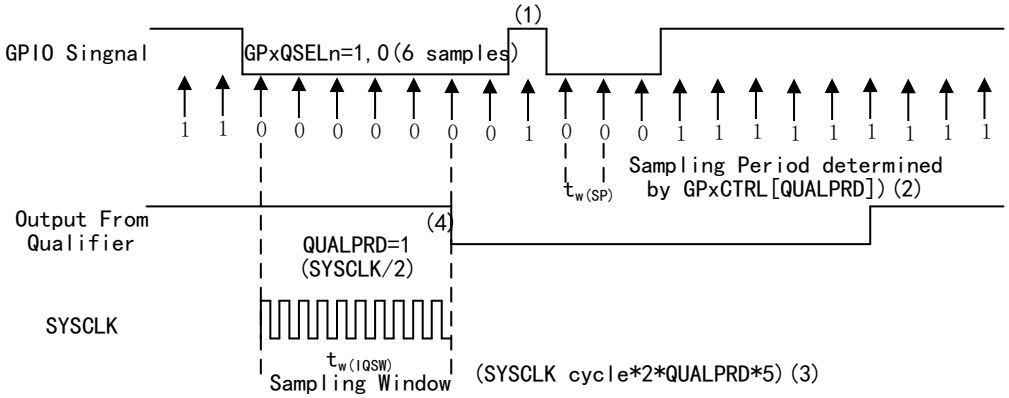
Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$t_{w(SP)}$	Sampling period	QUALPRD=0	$1t_{c(SYSCLK)}$		Cycle
		QUALPRD≠0	$2t_{c(SYSCLK)}$*QUALPRD		
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$*(n(1)-1)		Cycle
$t_{w(GPI)}$(2)	Pulse duration, GPIO low/high level	Synchronous mode	2tc（SYSCLK）		Cycle
		With input qualifier	$t_{w(IQSW)}$+ $t_{w(SP)}$+ $1t_{c(SYSCLK)}$		

Note:

(1) “n” represents the number of filtered samples defined by the GPxQSELn register.

(2) For $t_{w(GPI)}$, the pulse width is measured between VIL and VIL for low-level valid signals, and between VIH and VIH for high-level valid signals.

Figure 31 Sampling Mode



Note:

(1) The input filter will ignore this short-time pulse wave interference. QUALPRD bit field specifies the qualification sampling period. This bit field can vary between 00 and 0xFF. If QUALPRD=00, the sampling period is 1 SYSCLK period. For any other value of “n”, the qualification sampling period is 2n SYSCLK periods (namely, GPIO pins will be sampled every 2n SYSCLK periods).

(2) The qualification period selected through the GPxCTRL register will be applied to a group containing 8 GPIO pins.

(3) This filter can take 3 or 6 sampling values. GPxQSELn register selects the sampling mode to be used.

(4) In the examples, in order to enable the qualification window to detect changes, the input should remain stable for 10 SYSCLK periods or longer. In other words, the input should remain stable for (5 x QUALPRD x 2) SYSCLK periods. This will ensure that there are 5 sampling periods for detection. As external signals are asynchronously driven, the 13 SYSCLK-wide pulse ensures reliable recognition.

5.8.6.3. Sampling window width of input signals

The sampling frequency of the input signals represents the sampling frequency of a signal relative to SYSCLK, as shown below.

- If QUALPRD≠0, sampling frequency=SYSCLK/(2 × QUALPRD)
- If QUALPRD=0, sampling frequency=SYSCLK

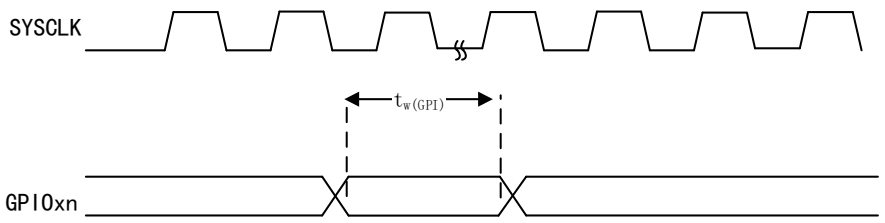
In the given sampling window, 3 or 6 sample values of the input signals are taken to determine the validity of the signals, which is determined by the values written to the GPxQSELn register. Refer to the previous section for general input timing requirements, and calculate the sampling window width of different modes as follows. Here tc(SYSCLK) represents the time period of SYSCLK.

There are two modes:

(1) When filtering with 3 sampling values
- If QUALPRD≠0, sampling window width = 2tc(SYSCLK)*QUALPRD*2
- If QUALPRD=0, sampling window width = tc(SYSCLK)*2

(2) When filtering with 6 sampling values
- If QUALPRD≠0, sampling window width = 2tc(SYSCLK)*QUALPRD*5
- If QUALPRD=0, sampling window width = tc(SYSCLK)*5

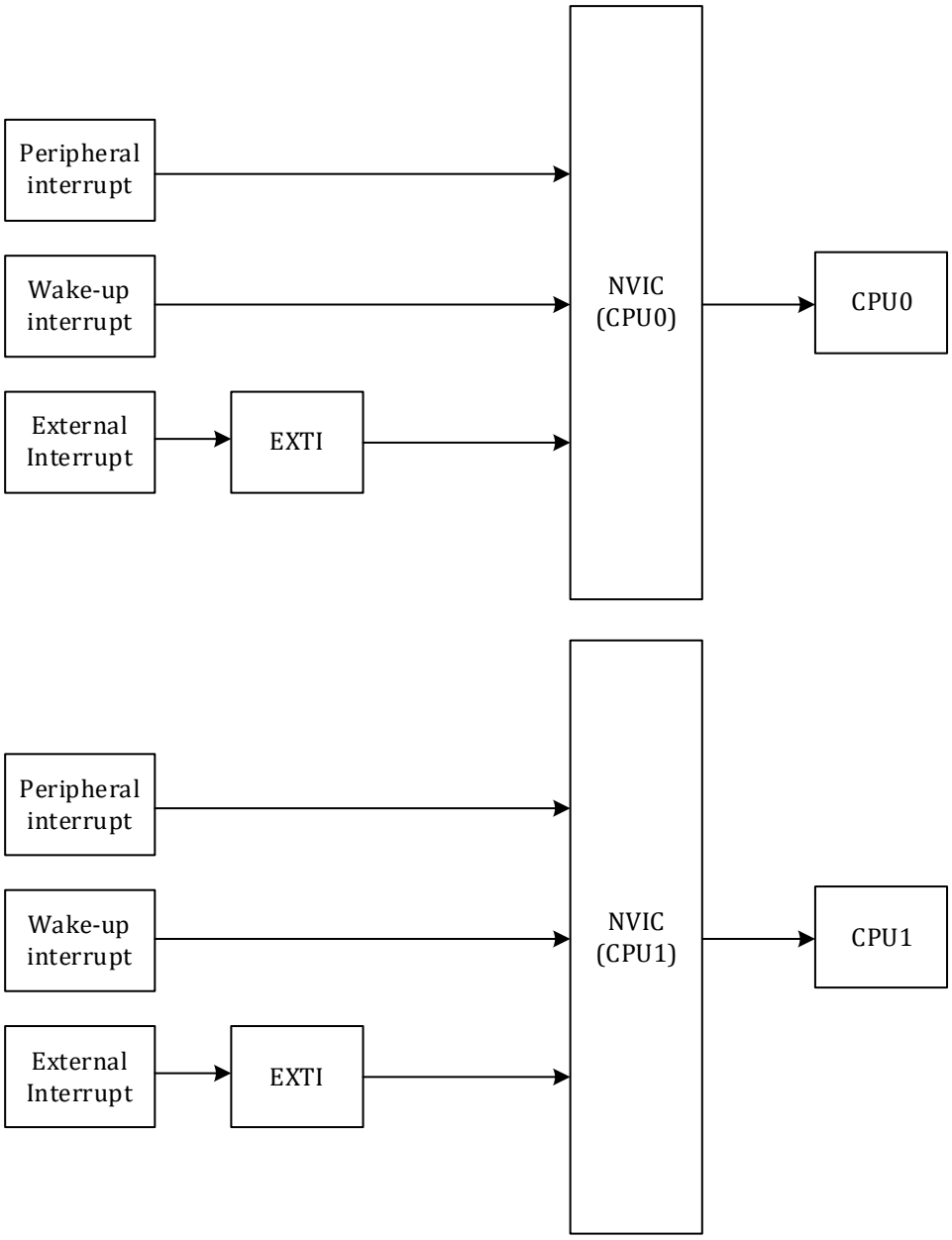
Figure 32 General-purpose Input Timing



5.8.7. Interrupt

The interrupt number for CPU0 and CPU1 of the device supports up to 226 interrupt lines, and all interrupts are sent to CPU through NVIC. This system provides a total of 16 external interrupts (GPIO/INPUT_XBAR) and peripheral interrupts (COMP).

Figure 33 Device Interrupt Architecture (EXTI)



5.8.7.1. Electrical data and timing of external interrupt (EXTI)

Table 78 External Interrupt Timing Requirements

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$t_{w(INT)}$	Pulse duration, INT input low/high level	Synchronous (1)	2tc（SYSCLK）		Cycle
		With the qualifier (2)	tw(IQSW)+ tw(SP)+ 1tc(SYSCLK)		

Note:

(1) The external inputs related to INPUT_XBAR of EXTI have synchronous or asynchronous function, and the signals given to EXTI by GPIO and COMP only support asynchronous trigger.

(2) For the description of input qualifier parameters, please refer to the table of "General-purpose Input Timing Requirements".

Table 79 External Interrupt Switch Characteristics

Parameter (1)			Minimum value	Maximum value	Unit
$t_{d(INT)}$	Delay time, time from INT low/high level to interrupt vector extraction (2)	Minimum value in the interrupt vector table that appears on the address line after the interrupt signal is set (3)	$t_{w(IQSW)}$+ 6$t_{c(SYSCLK)}$		Cycle
		Minimum value of the first instruction of executing the interrupt service routine after the interrupt signal is set (3)	$t_{w(IQSW)}$+ 18$t_{c(SYSCLK)}$		Cycle

Note:

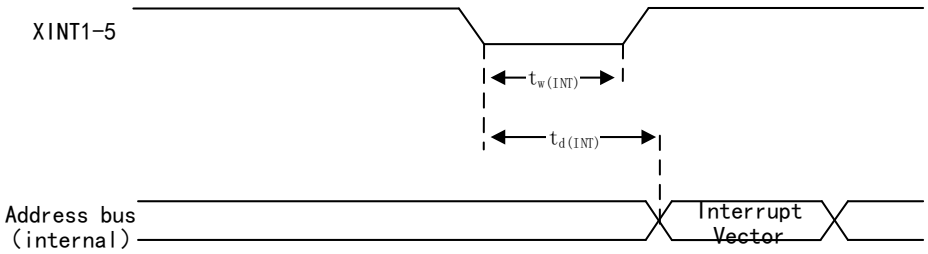
(1) For the description of input qualifier parameters, please refer to the table of "General-purpose Input Timing Requirements".

(2) This is based on the assumption that ISR is in a single-cycle memory.

(3) In this scenario, the value is measured without waiting delay for valuing, without waiting delay for bus access, and without any other interrupts.

(4) The CPU of this device supports interrupt nesting, interrupt preemption, and other operations, but the maximum value cannot be estimated. The minimum value under the condition of no interrupt nesting, no interrupt preemption, and no bus waiting is given in the table for reference.

Figure 34 External Interrupt Timing



5.8.8. Low-power mode

G32R5xx supports two clock gating low-power modes, i.e. halt and idle. These two low-power modes are entered by configuring the LPMCR register and executing WFI or WFE instructions. Besides, the SLEEPDEEP bit of the CPU SCB register needs to be configured according to the low-power mode.

Table 80 Clock Gating Low-power Modes

Module/Clock domain	Idle	Halt
SYSCLK	Active	Gating
CPU0_CLK	Gating	Gating
CPU1_CLK	Gating	Gating
APBCLK	Active	Gating

Module/Clock domain	Idle	Halt
WDTCLK	Active	Gating if CLKSRCTL1.WDHALTI = 0
PLL	Power-on	The software must power off the phase-locked loop before entering HALT.
INTOSC1	Power-on	Power off if CLKSRCTL1.WDHALTI = 0
INTOSC2	Power-on	Power off if CLKSRCTL1.WDHALTI = 0
XTAL(1)	Power-on	Power-on
FLASH(2)	Power-on	Power-on

Note:

(1) XTAL will not be powered off by hardware under any LPM. It can be powered off by setting XTALCR.OSCOFF bit to 1 through software. If XTAL is not required, this operation can be completed at any time in the application program.

(2) Flash module will not be powered off by hardware under any LPM. If the application needs it, it can be powered off by software.

5.8.8.1. Wake-up timing in low-power mode

Table 81 Timing Requirements of Idle Mode

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$t_{w(WAKE)}$	Pulse duration, external wake-up signal	Without the input qualifier(1)	2tc（SYSCLK）		Cycle
		With the input qualifier(1)	2tc (SYSCLK)+ tw (IQSW)		

Note:

(1) For the description of input qualifier parameters, please refer to the table of "General-purpose Input Timing Requirements".

Table 82 Idle Mode Switch Characteristics

Symbol	Parameter	Test conditions	Minimum value	Maximum value	Unit
td (WAKE-IDLE)	Delay time from external wake-up signal to program recovery execution (1)				Cycle
	Wake up from Flash Flash module in active state	Without the input qualifier(2)		53tc (SYSCLK)	
		With the input qualifier(2)		53tc (SYSCLK)+ tw (WAKE)	
	Wake up from RAM	Without the input qualifier(2)		39tc（SYSCLK）	
		With the input qualifier(2)		39tc (SYSCLK)+ tw (WAKE)	

Note:

(1) This time is the time when starting executing the instruction immediately after the IDLE instruction. The execution of ISR (triggered by wake-up signals) involves extra delay.

(2) For the description of input qualifier parameters, please refer to the table of "General-purpose Input Timing Requirements".

Figure 35 Entry and Exit Timing Diagram of Idle Mode

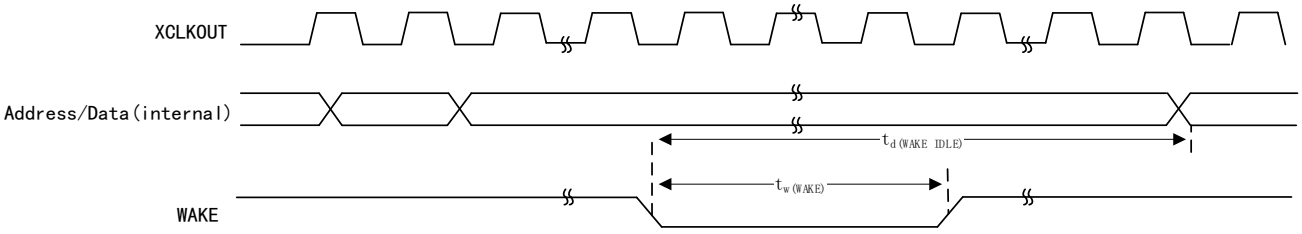


Table 83 Timing Requirements of Halt Mode

Symbol	Parameter	Minimum value	Maximum value	Unit
$t_{w(WAKE-GPIO)}$	Pulse duration, GPIO wake-up signal (1)	t_{oscst}+ 2$t_{c\ (OSCCLK)}$		Cycle
$t_{w(WAKE-XRS)}$	Pulse duration, XRSn wake-up signal (1)	t_{oscst}+8$t_{c(OSCCLK)}$		Cycle

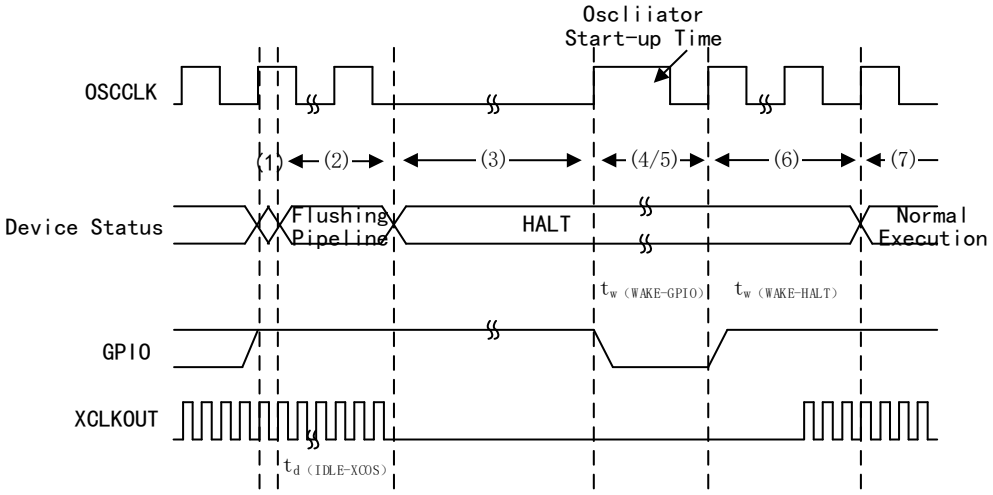
Note:

(1) If X1/X2 serves as OSCCLK, please refer to the startup time of specific oscillator provided by external circuit. Please refer to "Electrical Characteristics of Crystal Oscillators" for precautions. If INTOSC1 or INTOSC2 is used as OSCCLK, please refer to the information about toscst in "Internal Oscillators". The startup time of the oscillator is not suitable for applications using single-ended crystal oscillators on the X1 pin, as it is powered externally by the device.

Table 84 Halt Mode Switch Characteristics

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$t_{d(IDLE-XCOS)}$	Delay time from execution of IDLE instruction to stop of XCLKOUT	-	-	8$t_{c(OSCCLK)}$	Cycle
$t_{d(WAKE-HALT)}$	Delay time from the end of external wake-up signal to the restart of execution of CPU program	Wake up from Flash Flash module in activated state	-	1300$t_{c(OSCCLK)}$	Cycle
		Wake up from RAM	-	35$t_{c(OSCCLK)}$	

Figure 36 Entry and Exit Timing Diagram of Halt Mode



Note:

(1) Enter the halt mode by configuring the LPMCR register and executing the WFI or WFE instructions. Besides, the SLEEPDEEP bit of the CPU SCB register needs to be configured according to the low-power mode.

(2) The LPM block makes response to the HALT signal, and SYSCLK maintains a maximum of 8 OSCCLK clock cycles before shutdown (the actual cycle entering HALT mode is also affected by the bus/FLASH, and the number of cycles only considers the scenarios where other parts are idle). This delay makes the CPU pipeline and other pending operations refreshed correctly.

(3) The clock to the peripheral is disabled and PLL is turned off. If a quartz crystal oscillator or ceramic resonator is used as a clock source, the internal oscillator will also be turned off. Now the device is in halt mode and the power consumption is very low. The zero-pin internal oscillators (INTOSC1 and INTOSC2) and watchdog can be kept active in halt mode. To achieve this, it is necessary to write 1 to CLKSRCCTL1.WDHALTI. After the IDLE instruction is executed, a (minimum) delay of 5 OSCCLK periods is required before the wake-up signal takes effect.

(4) When the GPIOn pin (used to release the device from HALT mode) is driven to a low level, the oscillator will be turned on and the oscillator wake-up sequence will be activated. GPIO should be driven to high level only when the oscillator is stable. This provides a clean clock signal during the PLL sequence. As the falling edge of GPIO pin initiates wake-up process asynchronously, a low noise environment should be maintained before entering the halt mode and during this mode.

(5) The wake-up signal fed to the GPIO pin must meet the minimum pulse width requirement. In addition, this signal shall not have burrs. If a noise signal is fed to the GPIO pin, the wake-up behavior of the device will be uncertain and the device may not exit low-power mode in subsequent wake-up pulses.

(6) When the CLKIN of the core has been enabled, the device will respond to interrupts after some delay (if enabled). Now exit the halt mode.

(7) Restore normal operation.

(8) Users must relock the PLL during halt wake-up to ensure stable PLL locking.

5.9. Analog peripherals

The chip integrates high-performance analog units internally, including a 12-bit ADC, temperature sensor, DAC, and COMP. These analog units have the following characteristics

5.9.1. Main characteristics

Reference voltage of ADC:

- ADC takes VREFHIx and VREFLOx pins as reference
- The internal voltage reference range is 0V~3.3V or 0V~2.5V
- The voltage of VREFHIx pin is driven externally or generated by internal reference voltage

Pin reference for DAC:

- The buffer DAC takes VREFHIx and VSSA as reference or takes VDAC pin and VSSA as reference
- The comparator DAC takes VDDA and VSSA as reference or takes VDAC pins and VSSA as reference

Multiplexing function of the pin:

- Internally connected to VREFLO on all ADC, it can be used for bias self-calibration
- Buffer DAC output, comparator input and digital input are multiplexed with ADC input

Figure 37 Analog Subsystem Block Diagram (100-pin)

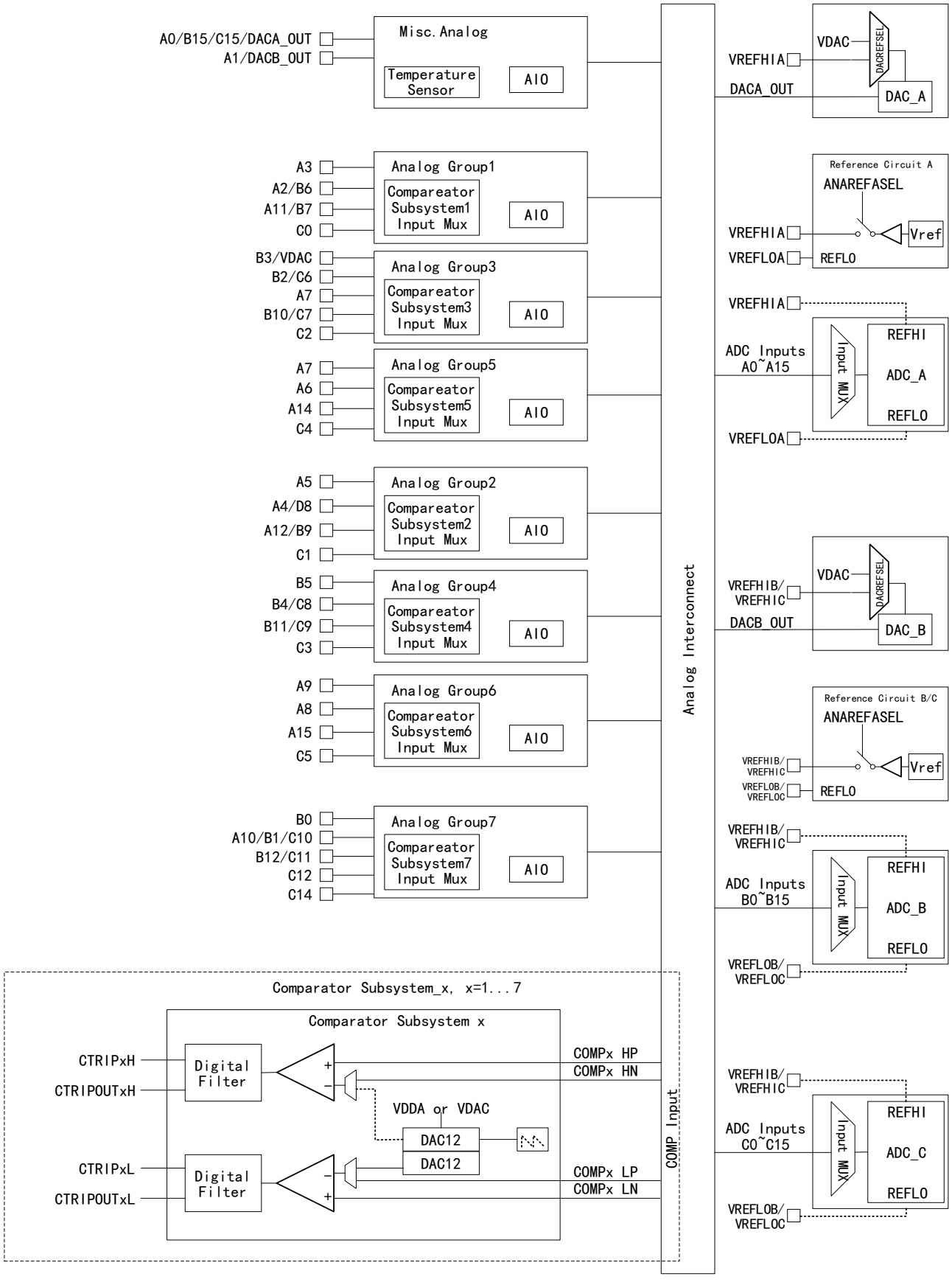


Figure 38 Analog Subsystem Block Diagram (80-pin)

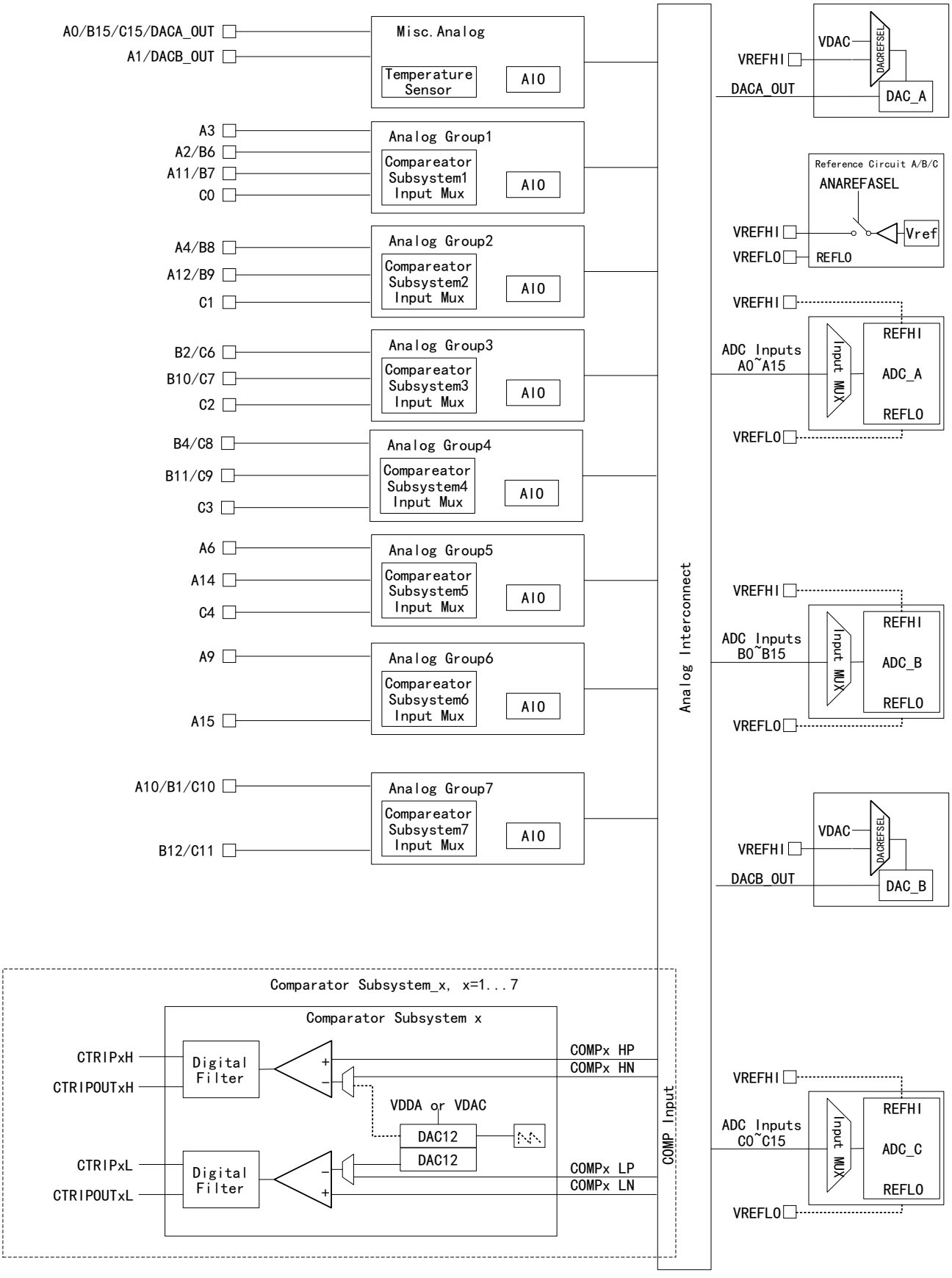


Figure 39 Analog Subsystem Block Diagram (64-pin)

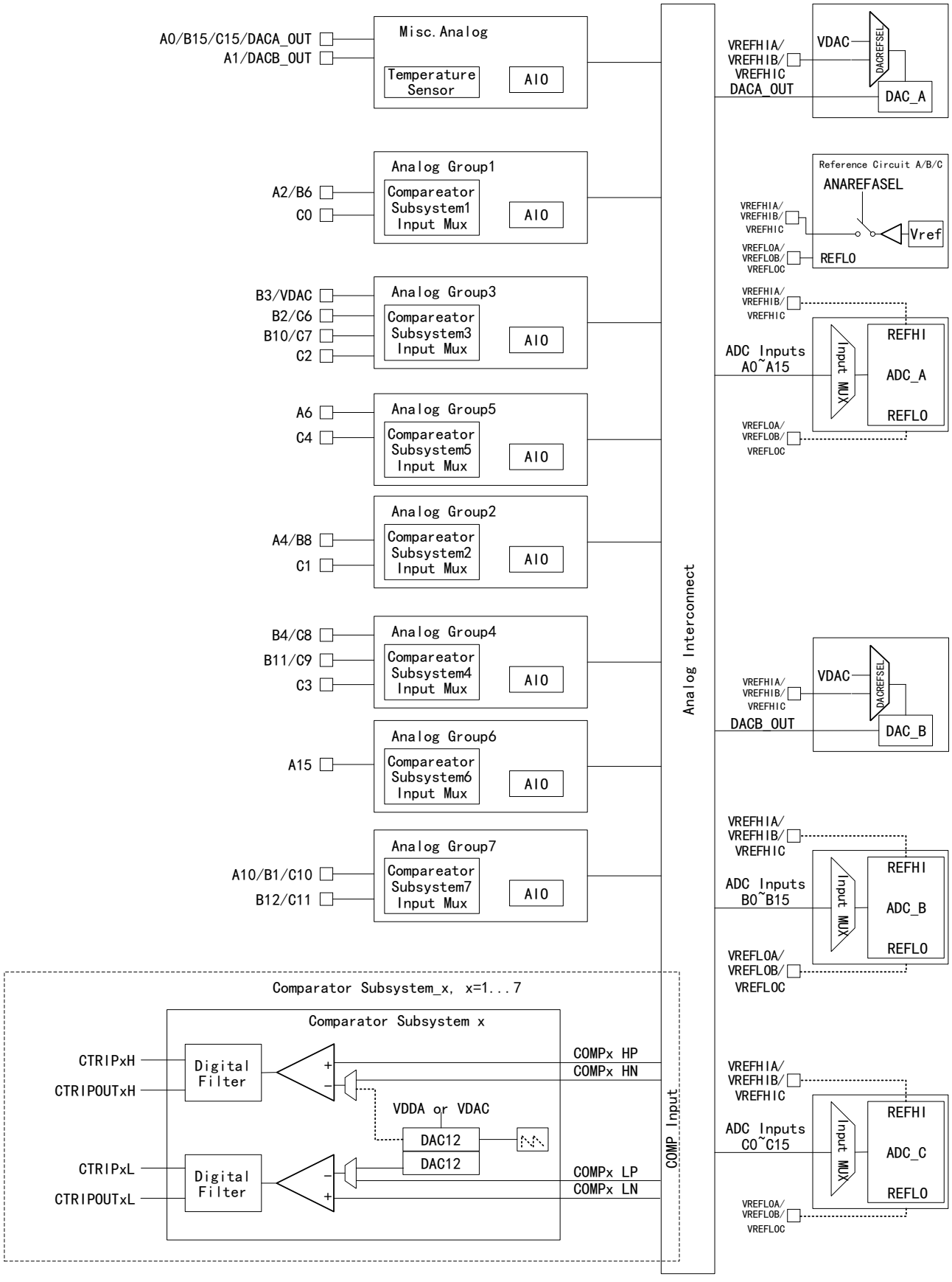


Figure 40 Analog Subsystem Block Diagram (56-pin)

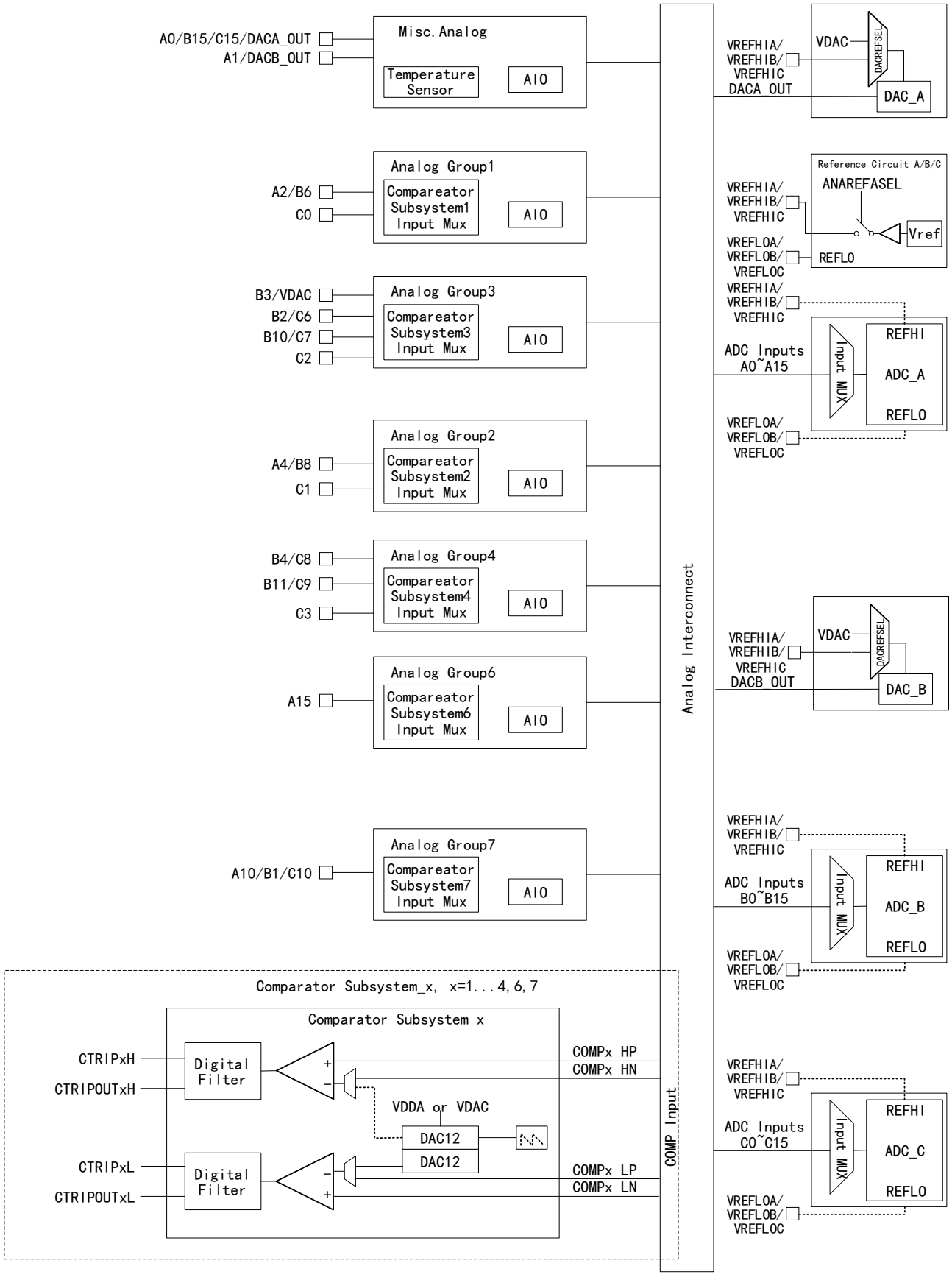
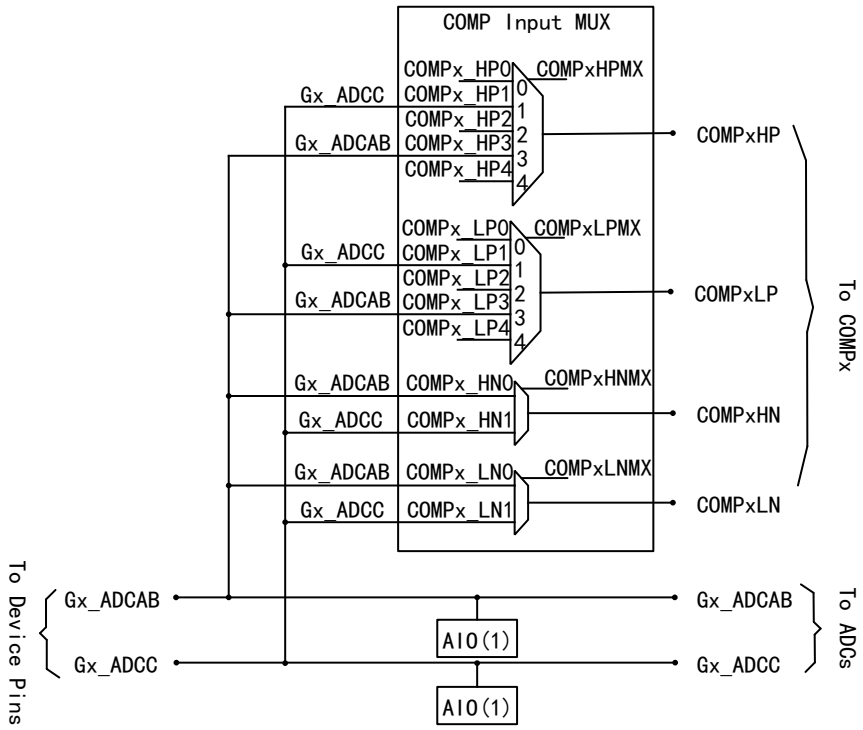


Figure 41 Analog Group Connection



Note:

(1) AIO only supports digital input mode.

Table 85 Analog Pins and Internal Connection

Pin name	Group name	Package				Always connected				Comparator				AIO
		LQFP 100	LQFP80	LQFP 64	QFN 56	ADC A	ADC B	ADC C	DAC	High positive (HPMXSEL)	High negative (HNMXSEL)	Low positive (LPMXSEL)	Low negative (LNMXSEL)	
VREFHIA	-	25	20(2) (VREFHI)	16(1)	14(1)									
VREFHIB	-	24(1)												
VREFHIC	-													
VREFLOA	-	27	21(2) (VREFLO)	17(1)	15(1)									
VREFLOB	-	26(1)												
VREFLOC	-													
Analog group 1										COMP1				
A3	G1_ADCAB	10	13			A3				3	0	3	0	AIO233
A2/B6		9	12	9	8	A2	B6			0		0		AIO224
A11/B7		18	16			A11	B7			2		2		AIO248
										4		4		
C0	G1_ADCC	19	16	12	10			C0		1	1	1	1	AIO237
Analog group 2										COMP2				
A5	G2_ADCAB	35				A5				3	0	3	0	AIO234
A4/B8		36	27	23	21	A4	B8			0		0		AIO225
A12/B9		30	22			A12	B9			2		2		AIO249
										4		4		
C1	G2_ADCC	29	22	18	16			C1		1	1	1	1	AIO238

Pin name	Group name	Package				Always connected				Comparator				AIO
		LQFP 100	LQFP80	LQFP 64	QFN 56	ADC A	ADC B	ADC C	DAC	High positive (HPMXSEL)	High negative (HNMXSEL)	Low positive (LPMXSEL)	Low negative (LNMXSEL)	
Analog group 3										COMP3				
B3/VDAC	G3_ADCAB	8		8	7		B3		VDAC	3	0	3	0	AIO242
B2/C6		7	11	7	6		B2	C6		0		0		AIO226
A7		20				A7				2		2		AIO235
B10/C7		15	14	10	9		B10	C7		4		4		AIO250
C2	G3_ADCC	21	17	13	11			C2		1	1	1	1	AIO244
Analog group 4										COMP4				
B5	G4_ADCAB	42					B5			3	0	3	0	AIO243
B4/C8		39	28	24	22		B4	C8		0		0		AIO227
B11/C9		13	13	10	9		B11	C9		4		4		AIO251
C3	G4_ADCC	31	23	19	17			C3		1	1	1	1	AIO245
										2		2		
Analog group 5										COMP5				
A7	G5_ADCAB	20				A7				3	0	3	0	AIO235
A6		6	10	6		A6				0		0		AIO228
A14		16	15			A14				4		4		AIO252
										2		2		
C4	G5_ADCC	17	15	11				C4		1	1	1	1	AIO239
Analog group 6										COMP6				

Pin name	Group name	Package				Always connected				Comparator				AIO
		LQFP 100	LQFP80	LQFP 64	QFN 56	ADC A	ADC B	ADC C	DAC	High positive (HPMXSEL)	High negative (HNMXSEL)	Low positive (LPMXSEL)	Low negative (LNMXSEL)	
A9	G6_ADCAB	38	28			A9				3	0	3	0	AIO236
A8		37				A8				0		0		AIO229
A15		14	14	10	15	A15				4		4		AIO253
C5	G6_ADCC	28						C5		1	1	1	1	AIO240
										2		2		
Analog group 7										COMP7				
B0	G7_ADCAB	41					B0			3	0	3	0	AIO241
A10/B1/C10		40	29	25	23	A10	B1	C10		0		0		AIO230
B12/C11		32	24	20	18		B12	C11		4		4		AIO254
C12	G7_ADCC	43						C12		2		2		AIO247
C14		44						C14		1	1	1	1	AIO246
Other analog														
A0/B15/C15/DACA_OUT		23	19	15	13	A0	B15	C15	DACA_OUT					AIO231
A1/DACB_OUT		22	18	14	12	A1			DACB_OUT					AIO232
	TempSensor(3)						B14							

Note: (1) After package, for LQFP100, VREFHIB and VREFHIC are the same pin in the pad, while VREFLOB and VREFLOC are the same pin in the pad; for LQFP64 and QFN56, VREFHIA, VREFHIB and VREFHIC are the same pin in the pad, while VREFLOA, VREFLOB and VREFLOC are the same pin in the pad

(2) For LQFP80, Pin20 is VREFHI, Pin21 is VREFLO.

(3) TempSensor is only for internal connection; and does not reach the device pin.

Table 86 Analog Signals

Signal name	Description
AIOx	Digital Input on ADC Pin
Ax	ADCA Input
Bx	ADCB Input
Cx	ADCC Input
VDAC	Optional External Reference Voltage for On-chip DAC. There is a 100pF VSSA capacitor on this pin, and neither the ADC input nor the DAC reference can be disabled. If it is used as the reference for on-chip DAC, place at least a 1μF capacitor on this pin.
DACx_OUT	Buffer DAC output
COMPx_DACH	High-level DAC Output of Comparator Subsystem
COMPx_DACL	Low-level DAC Output of Comparator Subsystem
COMPx_HPy	Positive Input of High-level Comparator of Comparator Subsystem
COMPx_HNy	Negative Input of High-level Comparator of Comparator Subsystem
COMPx_LPy	Positive Input of Low-level Comparator of Comparator Subsystem
COMPx_LNy	Negative Input of Low-level Comparator of Comparator Subsystem
TempSensor	Internal temperature sensor

5.9.2. Analog-to-digital converter (ADC)

The 12-bit precision ADC includes a wrapper and a core. The wrapper is based on the start of conversion (SOC) and consists of digital circuits that configure and control the ADC. These circuits include result registers, programmable conversion logic, analog circuit interfaces, peripheral bus interfaces, post-processing circuits, and other on-chip module interfaces. The core is made up of analog circuits, which include sampling/holding (S/H) circuits, successive approximation circuits, channel selection MUX, reference voltage circuits, and other analog support circuits. Each ADC module consists of a sampling/holding (s/h) circuit. Multiple ADC are allowed to sample simultaneously or operate independently.

5.9.2.1. Main characteristics

(1) Internal reference voltage options of ADC: 2.5V or 3.3V

(2) Single-ended conversion mode

(3) 12-bit precision resolution

(4) External reference is set by VREFHI and VREFLO pins

(5) Burst mode

(6) 16 result registers, which can be addressed separately

(7) 16-channel input multiplexer

(8) 16 configurable SOC

(9) Interrupt

- 4 NVIC interrupts
- Configurable interrupt layout

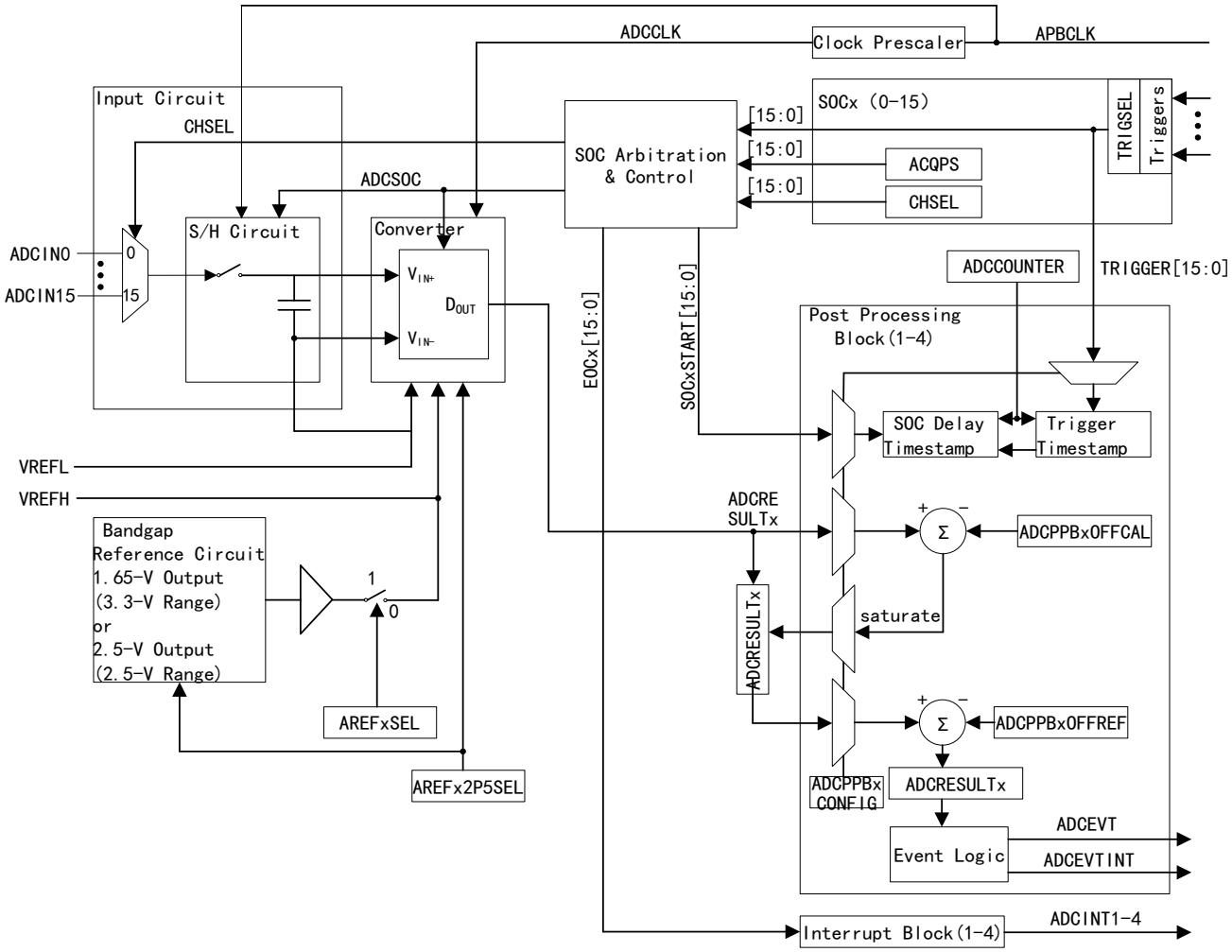
(10) Trigger source

- Software starts immediately
- TMR0/1/2
- ADCINT1/2
- GPIO ADCEXTSOC
- All PWM - ADCSOC A or B

(11) All the four post-processing blocks have:

- Saturation offset calibration
- Delay capture from trigger to sampling
- Set value calculation error
- High, low, and zero-crossing comparisons can trigger an interrupt or PWM

Figure 42 Structure Block Diagram



5.9.2.2. Result register mapping

The PPB result register is the calculation result of the ADC result obtained by setting the error correction value. When the error correction value is not set, the two values are equal. The bus controller includes CPU and DMA on specific device series and models. The result register read path is not supported and it can only be read through the APB bus. The CPU and DMA cannot access the ADC result register simultaneously.

5.9.2.3. ADC configuration

ADC configuration is divided into independent control by SOC and global control by each ADC module, as follows:

Table 87 ADC Options and Configuration

Option	Configuration
Resolution	Not configurable (only 12 bits)
Signal mode	Not configurable (single-ended only)
Conversion channel	SOC level
Trigger source	SOC level (1)
Sampling window duration	
EOC position	Module level
Burst mode	Module level (1)
Clock	
Reference voltage source	Module level (external or internal) (2)

Note:

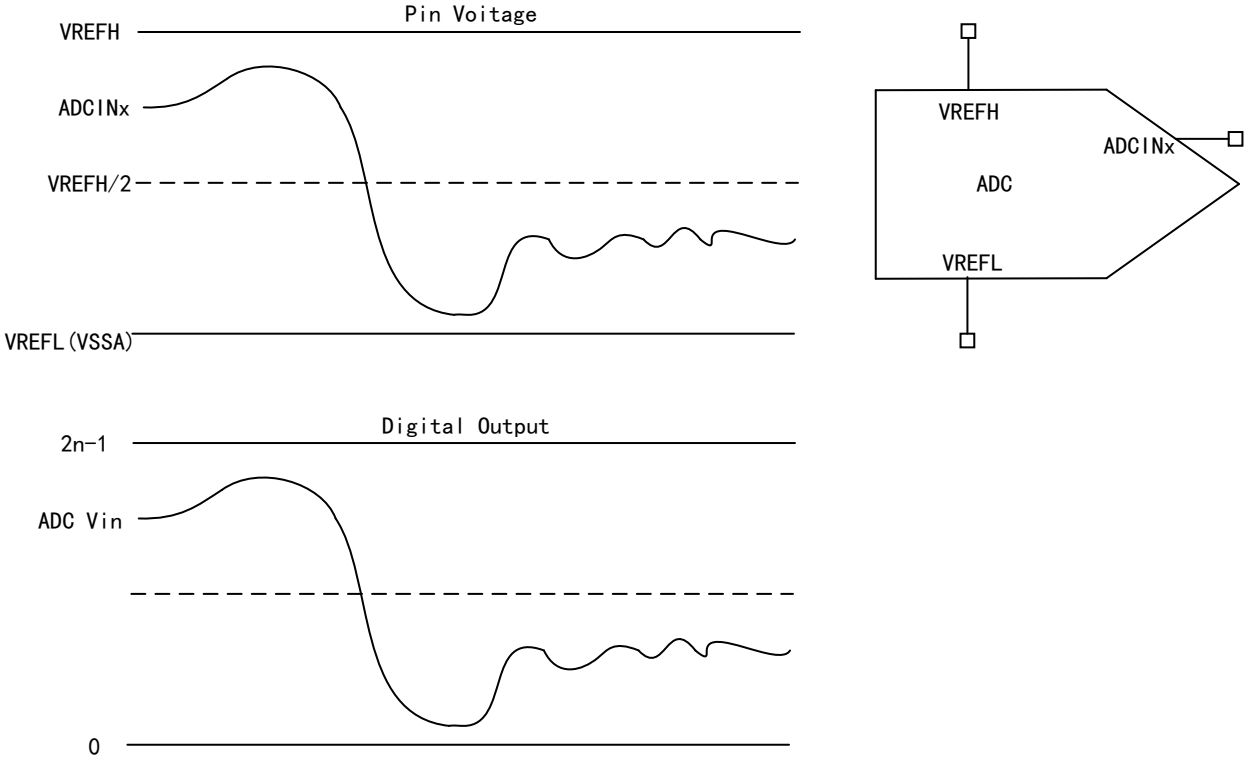
(1) In these configurations, writing different values to different ADC modules may result in asynchronous operation of the ADC.

(2) The low-pin number package may share one VREFHI pin among multiple ADC. At this time, the ADC that shares the reference pin must be configured with the same reference mode.

Signal mode

ADC supports single-ended signals. In single-ended mode, the input voltage of the converter is sampled through a pin ADCINx, with reference to VREFLO.

Figure 43 Single-ended Signal Mode



5.9.2.4. Electrical data and timing of ADC

5.9.2.4.1. Operating conditions of ADC

Table 88 Operating Conditions of ADC

Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
ADCCLK (1)		5		62.5	MHz
Sampling rate				3.45	MSPS
Sampling window duration (set by ACQPS and APBCLK) (2)	Rs with 50Ω or smaller	75			ns
VREFHI	External reference	2.4	2.5 or 3.0	V_{DDA}	V
VREFHI (3)	Internal reference voltage=3.3V range		1.65		V
	Internal reference voltage=2.5V range		2.5		V
VREFLO		VSSA	VSSA	VSSA	V
VREFHI - VREFLO	External reference	2.4		V_{DDA}	V
Conversion range	Internal reference voltage=3.3V range	0		3.3	V
	Internal reference voltage=2.5V range	0		2.5	V

	External reference	VREFLO		VREFHI	V

Note:

(1) Design reference value

(2) The sampling window must have a length of at least one ADCCLK cycle so as to ensure proper operation of the ADC.

(3) In internal reference mode, the reference voltage is driven by the device from the VREFHI pin. In this mode, users should not drive the voltage into the pins.

The ADC input should be kept below VDDA+0.3V. If the ADC input exceeds this threshold voltage, the internal VREF of the chip may be interfered with, thus affecting the results of other ADC or DAC input using the same VREF. The VREFHI pin must be kept below VDDA+0.3V so as to ensure its normal operation. If the VREFHI pin exceeds this threshold voltage, the blocking circuit may be activated, and the internal value of VREFHI may float to 0V internally, resulting in incorrect ADC conversion or DAC output.

5.9.2.4.2. Electrical characteristics of ADC

Table 89 General Characteristics

Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
ADCCLK conversion cycle	100MHz APBCLK	10.1		11	ADCCLK
Power-on time	External reference mode			500	μs
	Internal reference mode			5000	μs
	Use internal reference mode when switching between 2.5V and 3.3V			5000	μs
VREFHI input current (1)			130		μA
Internal reference capacitance value (2)		2.2			μF
External reference capacitance value (2)		2.2			μF

Note:

(1) When the ADC input is greater than VDDA, the load current on VREFHI will increase. This will result in inaccurate conversion.

(2) It is best to use the ceramic capacitors with a package size of 0805 or smaller. Tolerance of up to ±20% is acceptable.

Table 90 DC Characteristics

Parameter	**Test conditions**	**Minimum value**	**Typical value**	**Maximum value**	**Unit**
Gain error	Internal reference voltage	-45		45	LSB
	External reference		±3		

Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
Offset error			±2		
Gain error between channels			±2		
Offset error between channels			±2		
Gain error between ADC	All ADC have the same VREFHI and VREFLO		TBD		
Offset error between ADC	All ADC have the same VREFHI and VREFLO		TBD		
DNL error			TBD		
INL error			TBD		
Isolation between ADC	VREFHI=2.5V, synchronous ADC	-1.5	-	1.5	
	VREFHI=2.5V, asynchronous ADC	Not supported			

Table 91 AC Characteristics

Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
SNR (1)	VREFHI = 2.5V, fin = 100kHz, APBCLK from X1, ADC CLK =50MHz Fetch instructions from Flash via the CBUS interface, enabling CPU Cache and Flash prefetch.		66.2		dB
	VREFHI = 2.5V, fin = 100kHz, APBCLK from INTOSC, ADC CLK =50MHz		58.3		
THD (1)	VREFHI = 2.5V, fin = 100Hz, ADC CLK =50MHz Fetch instructions from Flash via the CBUS interface, enabling CPU Cache and Flash prefetch.		-74.1		dB
SFDR (1)	VREFHI = 2.5V, fin = 100kHz, ADC CLK =50MHz Fetch instructions from Flash via the CBUS interface, enabling CPU Cache and Flash prefetch.		76.4		dB
SINAD (1)	VREFHI = 2.5V, fin = 100kHz, APBCLK from X1, ADC CLK =50MHz Fetch instructions from Flash via the CBUS interface, enabling CPU Cache and Flash prefetch.		65.6		dB
	VREFHI = 2.5V, fin = 100kHz, APBCLK from INTOSC, ADC CLK =50MHz		58.6		dB
ENOB(1)	VREFHI = 2.5V, fin = 100kHz, APBCLK from X1, single ADC, ADCCLK =50MHz Fetch instructions from Flash via the CBUS interface, enabling CPU Cache and Flash prefetch.		10.5		Bit
	VREFHI = 2.5V, fin = 100kHz, APBCLK from X1, synchronous ADC, ADCCLK =50MHz		10.5		

Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
	VREFHI = 2.5V, fin = 100kHz, APBCLK from X1, asynchronous ADC, ADCCLK =50MHz		Not supported		
PSRR	VDD = 1.1V DC + 100mV DC to sine (at 1kHz), ADCCLK=50MHz		57		dB
	VDD = 1.1V DC + 100mV DC to sine (at 300kHz), ADCCLK=50MHz		57		
	VDDA = 3.3V DC + 200mV DC to sine (at 1kHz), ADCCLK=50MHz		58		
	VDDA = 3.3V DC + 200mV Sine (at 900kHz), ADCCLK=50MHz		57		

Note:

(1) As part of the best practice to reduce capacitive coupling and crosstalk, the IO activity on pins adjacent to the ADC input and VREFHI pin has been minimized.

5.9.2.4.3. ADC input model

Table 92 Editing Model Parameters

Symbol	Parameter	Reference mode	Value
Cp	Parasitic input capacitance	All	Please refer to the table below
Ron	Sampling switch resistance	External reference, 2.5V internal reference	500Ω
		3.3V internal reference	860Ω
Ch	Sampling capacitor	External reference, 2.5V internal reference	12.5pF
		3.3V internal reference	7.5pF
Rs	Nominal source impedance	All	50Ω

In single-ended operation, the input model needs to be used together with the actual signal source impedance so as to determine the sampling window duration.

Figure 44 Single-ended Input Model

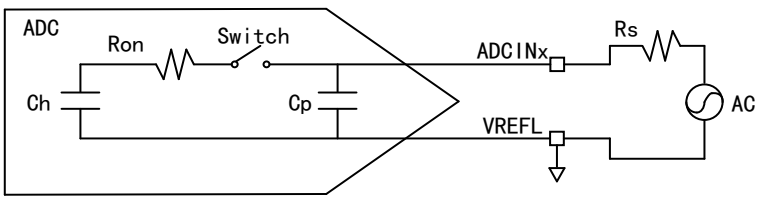


Table 93 Parasitic Capacitance of Each Channel

ADC channel	Cp (pF)	
	The comparator has been disabled	The comparator has been enabled
ADCINA0	12.7	15.2
ADCINA1	13.7	16.2
ADCINA2	9.2	11.7
ADCINA3	6.9	9.4
ADCINA4	9.2	11.7
ADCINA5	7.5	10
ADCINA6	8.0	10.5
ADCINA7	7.0	9.5
ADCINA8	10.0	12.5
ADCINA9	8.1	10.6
ADCINA10	9.3	11.8
ADCINB0	7.1	9.6
ADCINB1	9.3	11.8
ADCINB2	9.6	12.1
ADCINB3[1]	125.6	128.1
ADCINB4	8.8	11.3
ADCINB5	7.1	9.6
ADCINB6	9.2	11.7
ADCINB8	9.2	11.7
ADCINB15	12.7	15.2
ADCINC0	6.4	8.9
ADCINC1	6.1	8.6
ADCINC2	5.24	7.74
ADCINC3	5.5	8
ADCINC4	6.2	8.7
ADCINC5	5.6	8.1
ADCINC6	9.6	12.1
ADCINC8	8.8	11.3
ADCINC10	9.3	11.8
ADCINC12	4.1	6.6

ADC channel	Cp (pF)	
	The comparator has been disabled	The comparator has been enabled
ADCINC14	4.5	7
ADCINC15	12.7	15.2

Note:

(1) This pin is also used to provide reference voltage for COMPDAC and GPDAC, and includes an internal decoupling capacitor.

5.9.2.4.4. ADC Timing Diagram

The ADC conversion timing of two SOC in the following situations:

- SOC0 and SOC1 use the same trigger
- The round robin pointer points to SOC0 and it converts first
- When a trigger occurs, no other SOC is converting or hanging
- ADCINTSEL is configured to set the ADCINTx flag at the end of SOC0 conversion

Figure 45 ADC Timing

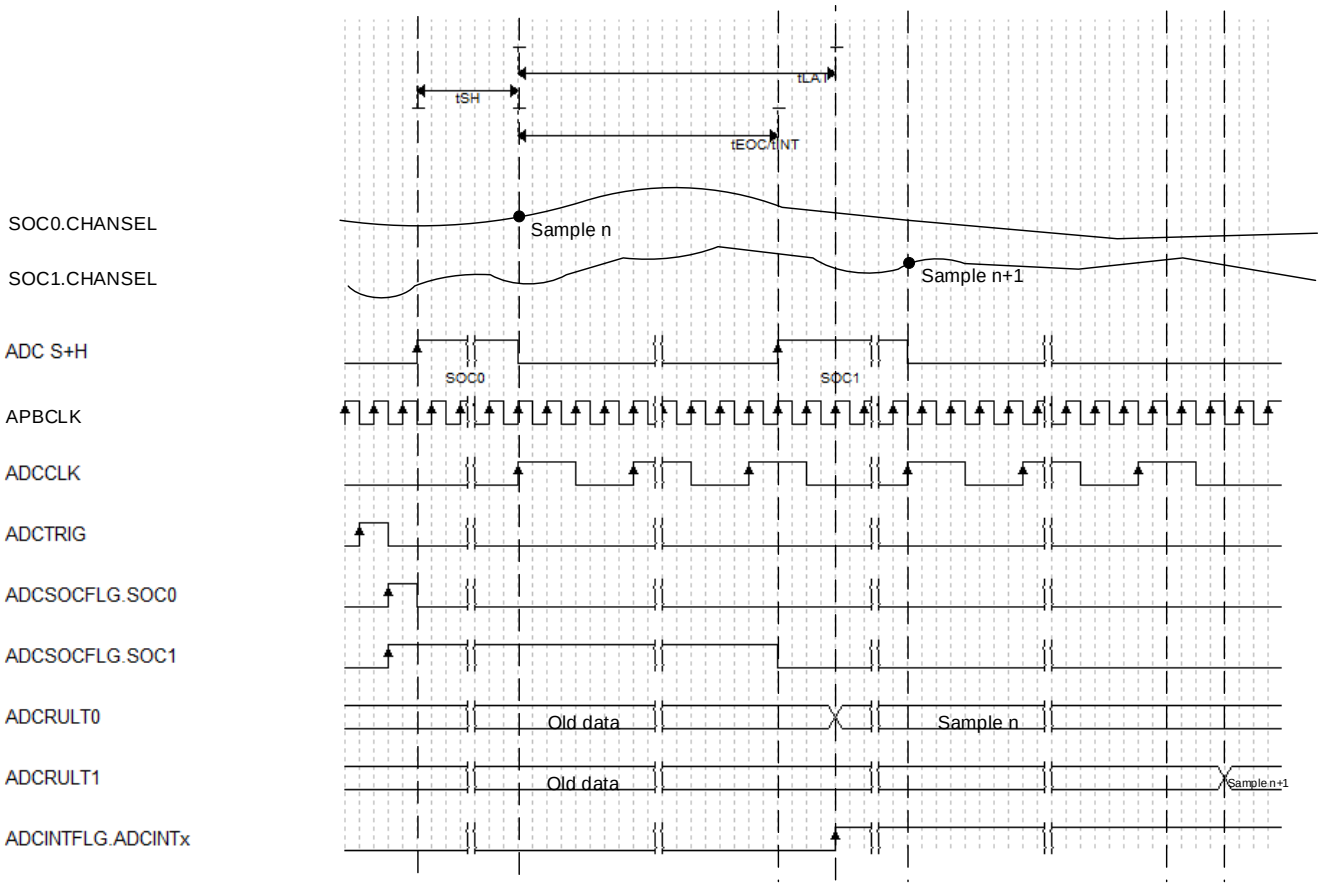


Table 94 ADC Timing Parameters

Parameter	Description
t_{SH}	Duration of S+H window. At the end of this window, the value on the S+H capacitor becomes the voltage to be converted into a digital value. The duration is calculated from (ACQPS+1) APBCLK cycles. ACQPS can be configured separately for each SOC, so t_{SH} may not be the same for different SOC. Note: No matter how the chip clock is set, the value of the S+H capacitor will be captured approximately 5ns before the end of the S+H window.
t_{LAT}	The duration from the end of the S+H window to the time of latching the ADC result to the ADCRESULTx register. Note: If the ADCRESULTx register is read before this time, the previous conversion result will be returned.
t_{EOC}	The duration from the end of the S+H window to the time when the S+H window of the next ADC conversion can start. Subsequent sampling can begin before the conversion result is latched.
t_{INT}	The duration from the end of the S+H window to the setting of the ADCINT flag (provided that the ADCINT flag has been configured). If the INTPULSEPOS bit in the ADCCTL1 register is set, t_{INT} will be consistent with the conversion result latched to the result register. When the INTPULSEPOS bit is set to 0, t_{INT} will be consistent with the end of the S+H window. If tINT triggers reading of the ADC result register (reading directly through DMA or indirectly through triggering the ISR of read result), read after the result is latched; otherwise, the read value will be the previous result. When the INTPULSEPOS bit is 0 and the OFFSET field in the ADCINTCYCLE register is not 0, there will be a delay of OFFSET APBCLK cycles before setting the ADCINT flag. This delay can be used to enter ISR or trigger DMA when sampling is ready.

Table 95 ADC Timing for 12-bit Mode

ADCCLK prescale		**APBCLK cycle**				**ADCCLK cycle**
Prescale ratio	PRESCALE	t_{LAT}(1)	t_{EOC}	t_{INT}(early stage)(2)	t_{INT} (later stage)	t_{EOC}
1	0	13	11	1	11	11
2	2	23	21	1	21	10.5
3	4	34	31	1	31	10.3
4	6	44	41	1	41	10.3
5	8	55	51	1	51	10.2
6	10	65	61	1	61	10.2
7	12	76	71	1	71	10.1
8	14	86	81	1	81	10.1

Note:

(1) Please refer to the announcement of "ADC: DMA Reads Outdated Results"

(2) By default, if INTPULSEPOS is 0, t_{INT} occurs within one APBCLK cycle after the S+H window. This can be changed by writing to the OFFSET field of the ADCINTCYCLE register.

5.9.3. Temperature sensor

The temperature sensor can be used to measure the junction temperature of the device. The temperature sensor is sampled through internal connection with the ADC, and it is converted into temperature through software. When sampling the temperature sensor, ADC must meet the following requirements for acquisition time.

Table 96 Characteristics of Temperature Sensor

Symbol	Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
T_{acc}	Temperature accuracy	External reference		±15		°C
$t_{startup}$	Startup time (From TSNSCTL [ENABLE] to sampling temperature sensor)			500		μs
t_{SH}	ADC sampling holding time		450			ns

5.9.4. Buffer digital-to-analog converter (DAC)

The buffer DAC is a universal DAC, and it consists of an internal 12-bit DAC and an analog output buffer that can drive external loads. It can generate AC waveforms such as sine waves, square waves, and triangular waves, as well as DC voltages. Writing software to the DAC value register can take immediate effect or be synchronized with EPWMSYNCO events.

5.9.4.1. Main characteristics

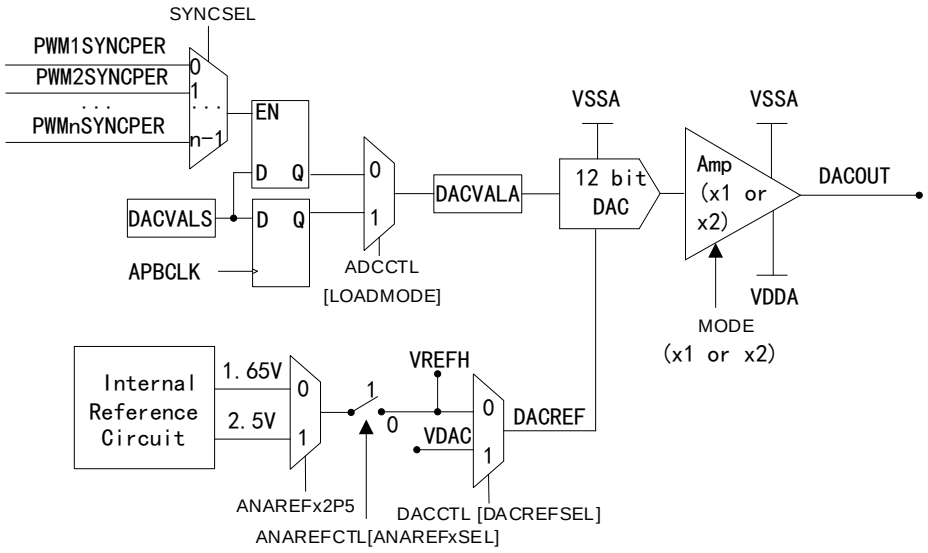
(1) Resolution: 12 bits

(2) Optional reference voltage source

(3) Can synchronize with PWMSYNCPER

(4) In x1 and x2 mode, use the internal VREFHI

Figure 46 Structure Block Diagram



5.9.4.2. Electrical data and timing of buffer DAC

5.9.4.2.1. Operating conditions of buffer DAC

Table 97 Operating Conditions of Buffer DAC

Symbol	Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
R_L	Resistive load (1)		5			kΩ
C_L	Capacitive load				100	pF
V_{OUT}	Effective output voltage range (2)	R_L = 5kΩ	0.3		VDDA – 0.3	V
		RL = 1kΩ	0.6		VDDA – 0.6	V
Reference voltage (3)		VDAC or VREFHI	2.4	2.5 or 3.0	V_{DDA}	V

Note: The typical values are measured when VREFHI = 3.3V and VREFLO = 0V; the minimum and maximum values are measured when VREFHI = 2.5V and VREFLO = 0V.

(1) DAC can drive the resistive loads with a minimum value of 1kΩ, but the output range will be limited under these conditions.

(2) V_{OUT} represents the linear output range of DAC. DAC can generate voltages beyond this range, but due to the buffer, the output voltage will not be linear under these conditions.

(3) To achieve excellent PSRR performance, be sure VDAC or VREFHI is less than VDDA.

5.9.4.2.2. Electrical characteristics of buffer DAC

Table 98 General Characteristics

Symbol	Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
	Resolution		12			Bit

Symbol	Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
	Load regulation		-0.5		-0.5	mV/V
	Burr pulse energy			0.5		V-ns
	Full range of voltage output stability time	Stable to 2LSB after switching from 0.3V to 3V			2	μs
	1/4 full scale of voltage output stability time	Stable to 2LSB after switching from 0.3V to 0.75V			1	μs
	Voltage output slew rate	Slew rate of converting from 0.3V to 3V	7.8		15.5	V/μs
	Stability time of load transient (1)	5kΩ load			350	ns
		1kΩ load			557	ns
	Reference input resistance (2)	VDAC or VREFHI	160	200	240	kΩ
TPU	Power-on time	External reference mode			500	μs
		Internal reference mode			5000	μs

Note: The typical values are measured when VREFHI = 3.3V and VREFLO = 0V; the minimum and maximum values are measured when VREFHI = 2.5V and VREFLO = 0V.

(1) Stable within 3 LSB.

(2) Each active buffer DAC module.

Table 99 DC Characteristics

Symbol	**Parameter**	**Test conditions**	**Minimum value**	**Typical value**	**Maximum value**	**Unit**
	Offset error	Midpoint	-8		8	mV
Gain	Gain error (1)		-2.5		2.5	FSR percentage
DNL	Differential nonlinearity (2)	Corrected endpoint	-1	±0.6	1	LSB
INL	Integral nonlinearity	Corrected endpoint	-5	±2	5	LSB

Note:

(1) The gain error is calculated within the linear output range.

(2) DAC output is monotonic output.

Table 100 AC Characteristics

Symbol	Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
	Output noise	Integral noise from 100Hz to 100kHz		TBD		μVrms
		Noise density at 10kHz		TBD		nVrms/√Hz

Symbol	Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
SNR	Signal-to-noise ratio	2.34375kHz, 200KSPS		TBD		dB
THD	Total harmonic distortion	2.34375kHz, 200KSPS		TBD		dB
SFDR	Spurious-free dynamic range	2.34375kHz, 200KSPS		TBD		dB
SINAD	Signal-to-noise ratio and distortion ratio	2.34375kHz, 200KSPS		TBD		dB
PSRR	Power supply rejection ratio (1)	DC		70		dB
		100kHz		30		dB

Note:

(1) VREFHI = 3.2V, VDDA = 3.3V DC + 100mV sine.

To ensure normal operation of the chip, the VDAC pin must be maintained below VDDA+0.3V. If the VDAC pin exceeds this level, the blocking circuit may be activated, and the internal value of VDAC may float to 0V internally, resulting in incorrect DAC output. The VREFHI pin must be kept below VDDA+0.3V so as to ensure its normal operation. If the VREFHI pin exceeds this level, the blocking circuit may be activated, and the internal value of VREFHI may float to 0V internally, resulting in incorrect ADC conversion or DAC output.

5.9.4.2.3. Buffer DAC Diagram

Figure 47 Offset of Buffer DAC

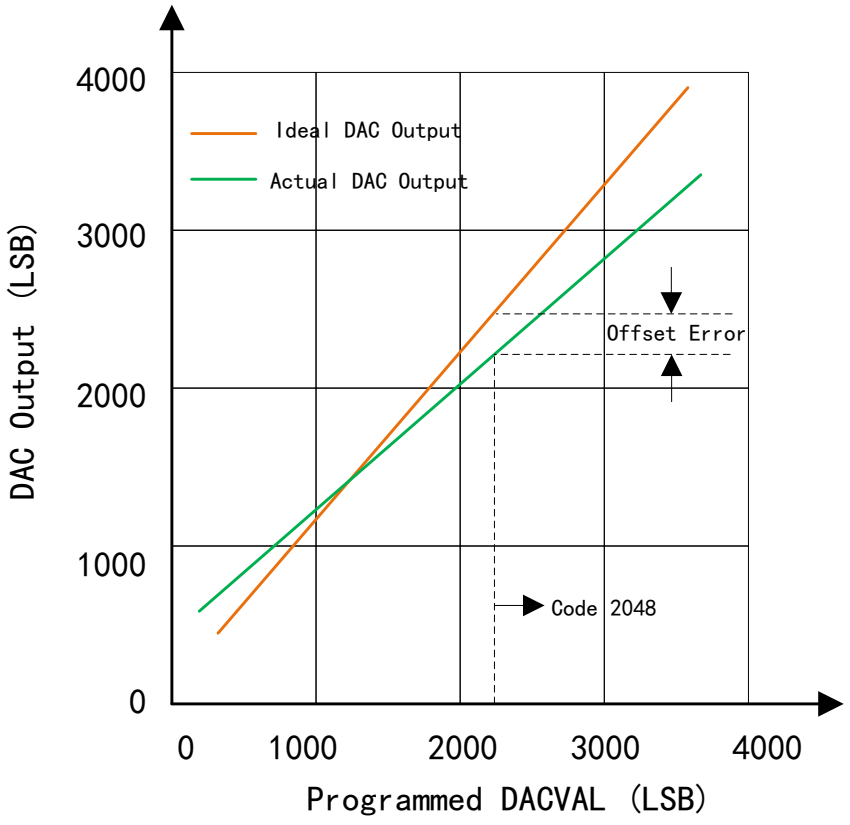


Figure 48 Gain of Buffer DAC

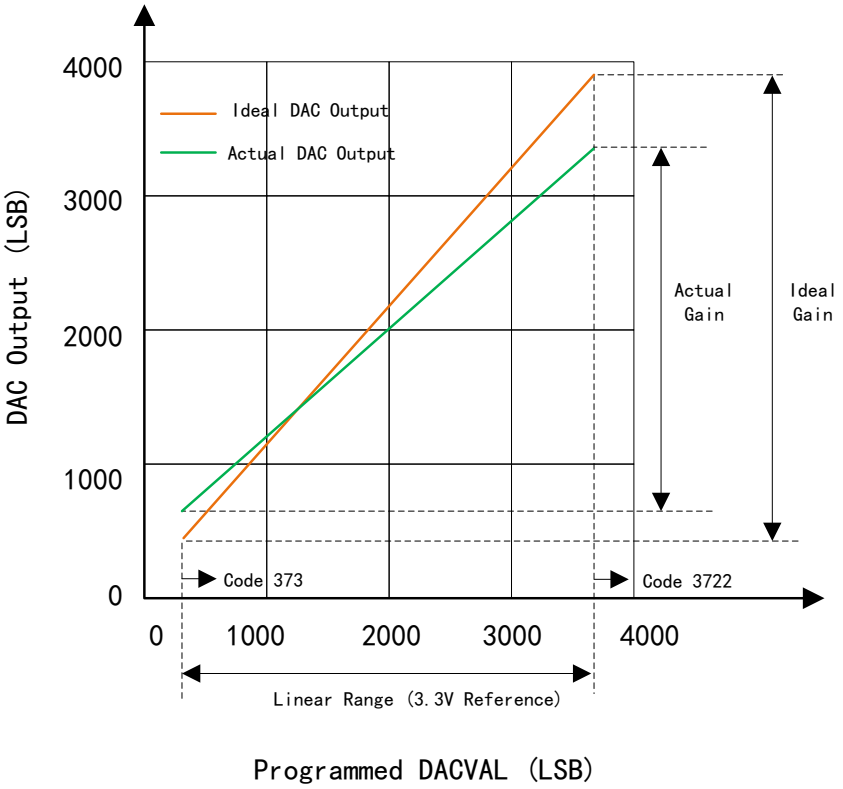
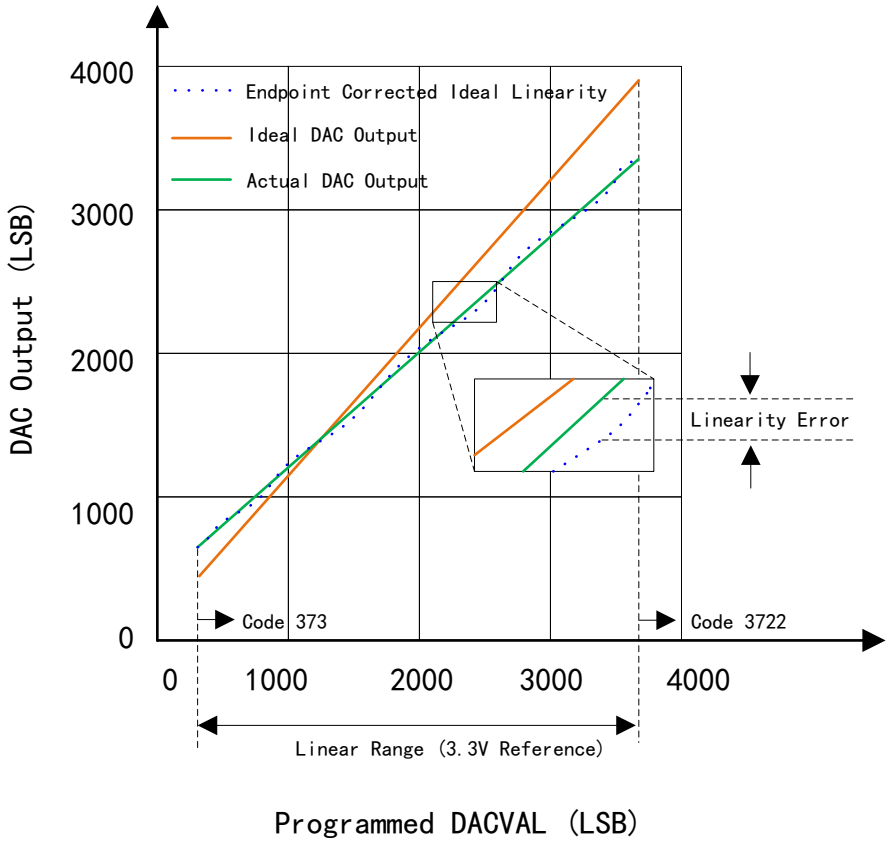


Figure 49 Linearity of Buffer DAC



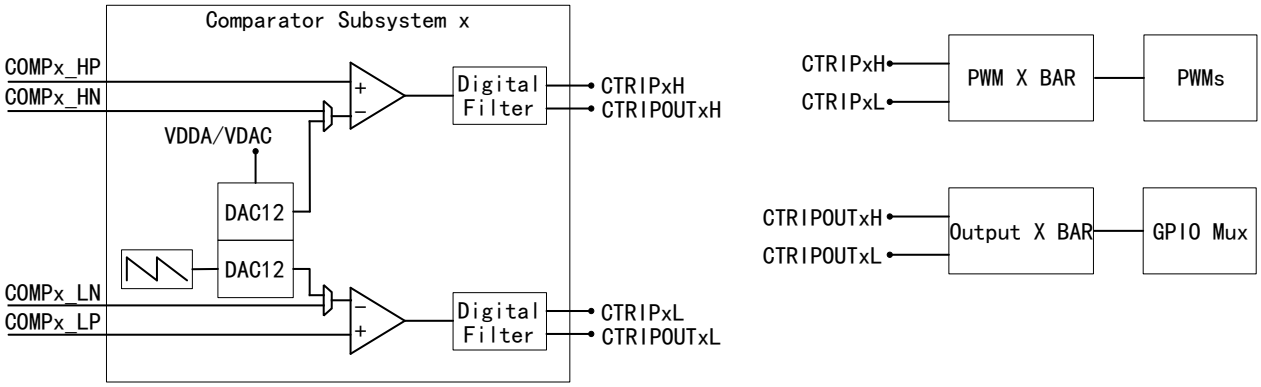
5.9.5. Comparator (COMP)

Each COMP system includes two comparators, two reference 12-bit DAC, two digital filters, and a ramp generator.

As shown in the figure below, the comparator uses "H" to represent high level and "L" to represent low level in each module. Each comparator can generate a digital output, indicating whether the voltage on the positive input is greater than the voltage on the negative input. The positive input of the comparator can be driven by external pins, while the negative input is driven by external pins or programmable reference 12-bit DAC. Each comparator output will pass through a programmable digital filter, which can remove the pseudo jump signals. If filtering is not needed, unfiltered output can be used.

The ramp generator circuit can be used to control the reference 12-bit DAC values of the high-level comparator in the subsystem. Each COMP module has two outputs. These two outputs are connected to the PWM module or GPIO pin after passing through the digital filter and XBAR.

Figure 50 COMP Connection



Note: In the figure, x=1-7, and not all packages have all COMP pins. Please refer to the table of "Analog Pins and Internal Connection".

5.9.5.1. Electrical data and timing of COMP

5.9.5.1.1. Electrical characteristics of comparators

Table 101 Electrical Characteristics

Symbol	Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
TPU	Power-on time				500	μs
	Range of comparator input (COMPINxx)		0		V_{DDA}	V
	Offset error based on input	Low common mode, with reverse input set to 50mV	-20		20	mV
	Hysteresis (1)	1x		12		LSB
		2x		24		
		3x		36		
		4x		48		
	Response time (delay of change from COMPINx input to PWM X-BAR output or X-BAR output)	Step response		21	60	ns
		Slope response (1.65V/μs)		26		
		Slope response (8.25mV/μs)		50		ns
PSRR	Power supply rejection ratio	Up to 250kHz		46		dB
CMRR	Common-mode rejection ratio		40			dB

Note:

(1) COMP DAC is used as a reference to determine how much hysteresis is applied. Therefore, hysteresis will vary with the COMP DAC reference voltage. Hysteresis applies to configurations of all comparator input sources.

To ensure normal operation of the chip, the COMP input must be maintained below VDDA+0.3V. If the COMP input exceeds the threshold voltage, the internal blocking circuit will cause the internal comparators to be isolated from the external pins until the external pin voltage returns to below the threshold voltage. During this period, the internal comparator input will be in a suspended state and can attenuate to below VDDA within approximately 0.5μs. After that, the comparator may start outputting incorrect results, depending on the values input by other comparators.

Figure 51 Offset of COMP Comparators Based on Input

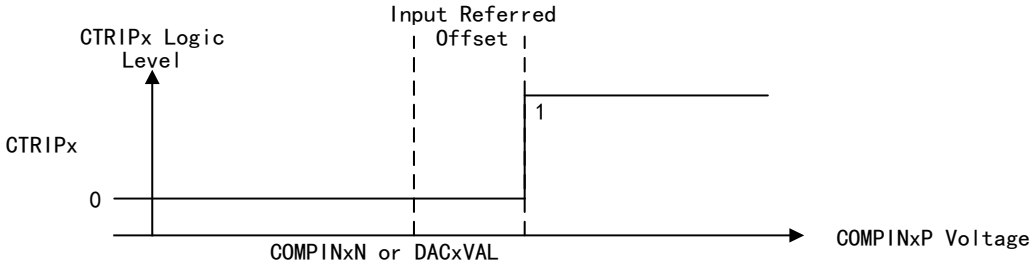


Figure 52 COMP Comparator Hysteresis

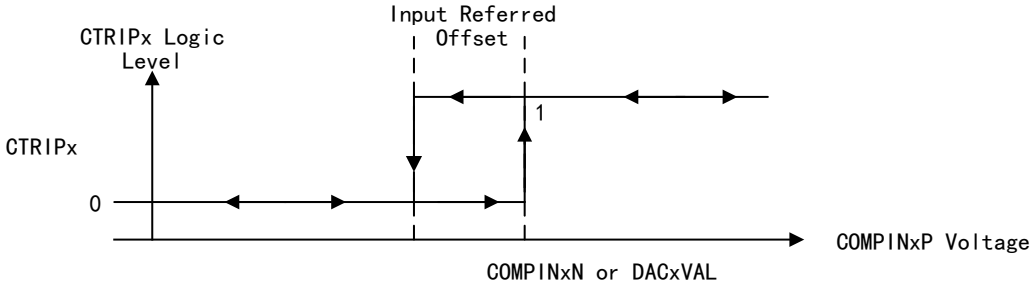


Table 102 COMP DAC Static Electrical Characteristics

Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
COMP DAC output range	Internal reference	0		V_{DDA}	V
	External reference	0		VDAC(4)	
Static offset error (1)		-25		25	mV
Static gain error (1)		-2		2	FSR percentage
Static DNL	Corrected endpoint	>-1		4	LSB
Static INL	Corrected endpoint	-16		16	LSB
Settling time	Stabilize to 1LSB after full-range output changes			1	μs

Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
Resolution			12		Bit
COMP DAC output interference (2)	Errors caused by comparator tripping or COMP DAC code changes within the same COMP module	-100		100	LSB
COMP DAC interference time (2)				200	ns
VDAC reference voltage	When VDAC is used as the reference	2.4	2.5 or 3.0	V_{DDA}	V
VDAC load (3)	When VDAC is used as the reference	6	8	10	kΩ

Note:

(1) It contains errors based on the comparator input.

(2) During a period of time after the comparator trips, there may be interference errors in the COMP DAC output.

(3) Each active COMP module.

(4) When VDAC>VDDA, the maximum output voltage is VDDA.

5.9.5.1.2. COMP Schematic Diagrams

Figure 53 Static Offset of COMP DAC

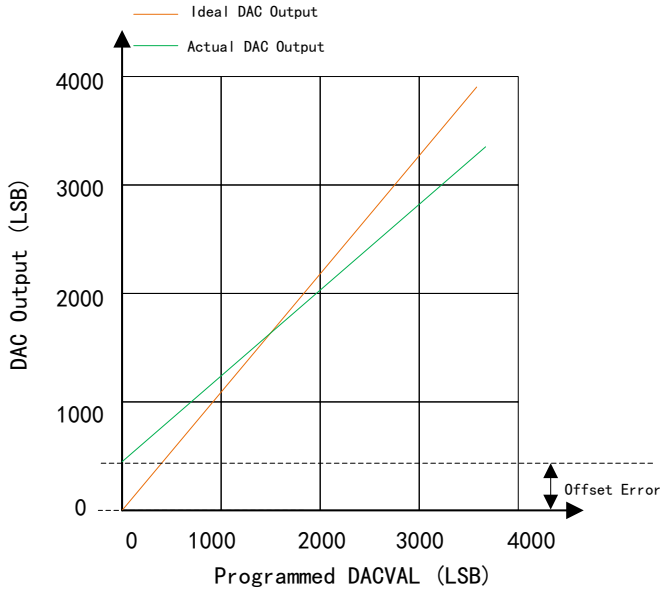


Figure 54 Static Gain of COMP DAC

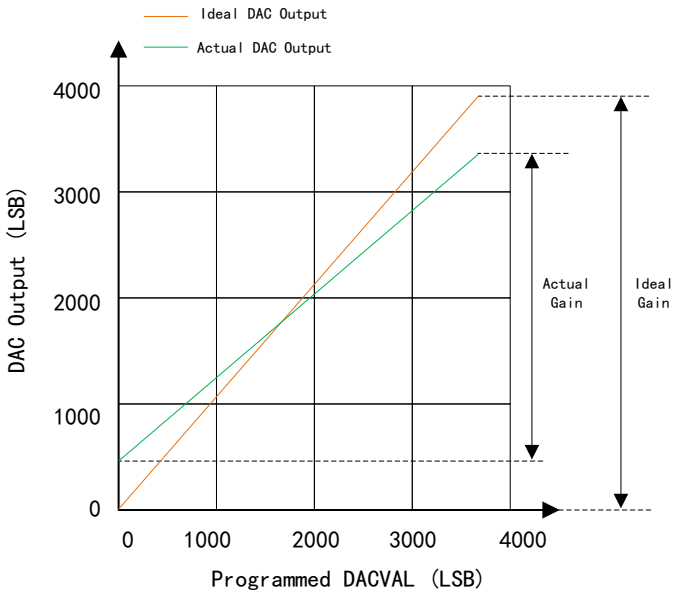
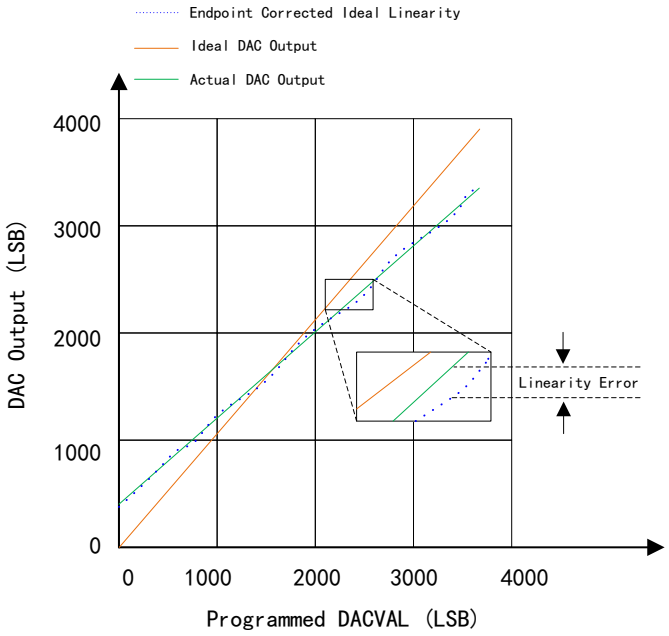


Figure 55 Static Linearity of COMP DAC



5.10. Control peripherals

5.10.1. Capture (CAP)

The capture is used in systems for accurately timing the external events. The capturer can decode the voltage or current amplitude from the duty cycle code current/voltage sensor, and measure the duty cycle and period of the pulse sequence signal, and the elapsed time between position sensor pulses. It supports measurement of the speed of rotating machinery through the toothed chain wheels sensed by Hall sensors.

5.10.1.1. Main characteristics

(1) 128:1 input multiplexer

(2) Event filter prescale

(3) 4 32-bit event timestamp registers

(4) Capture up to four timestamp events at a time

(5) Capture the timestamps in a four-depth circular buffer through continuous mode

(6) Used in edge polarity selection for up to four sequence timestamp capture events

(7) Can respond to any of the four events and generate interrupts

(8) Differential (Delta) mode timestamp capture

(9) Absolute timestamp capture

(10) Independent DMA trigger

(11) CAP can be configured as a single-channel PWM output (when CAP is not used for input capture)

(12) Type 1 CAP additionally has the following functions compared with Type 0 CAP:

- WRPRT protection (already added to key registers)
- Input multiplexer
  - Select the capture input source according to ECCTL0[INPUTSEL] bit; for details, please refer to Multiplexer Configuration.
- Modulo counter status bit
  - In Type 0 CAP, the current state of the modulo counter cannot be known. However, in Type 1 CAP, the ECCTL2[MODCNTRSTS] bit can indicate which capture register to load in next capture event.
- Event filter reset
  - Reset can be used for initialization and debugging. The modulo counter, event filter, and any pending interrupt flags can be cleared by setting the ECCTL2[CTRFILTRESET] bit.
- DMA trigger source
  - CAPxDMA is a DMA trigger. The DMA interrupt source can be selected as CEVTx (x=1... 4) through ECCTL2[DMAEVTSEL].

(13) Each CAP channel has the following functions:

- 128:1 input multiplexer
- Connect the capture input using the input X-BAR
- In APWM mode, the output X-BAR is configured as output
- Input capture signal prescale
- Select the independent edge polarity (rising edge/falling edge) for four capture events
- 4 32-bit timestamp registers
- 32-bit counter

- A four-order sequencer (modulo-4 counter) synchronized with external events, rising/falling edge of the CAP pin
- WRPRT protection
- Independent DMA trigger
- Interrupt function for any of the four capture events
- It can reset the modulo counters, event filters, and interrupt flags
- Control the continuous timestamp capture in a four-depth ring buffer
- The status register of the modulo counter is used to indicate the current status of the modulo counter
- Trigger the compare registers (two bits) once, and freeze 1-4 timestamp events after capture

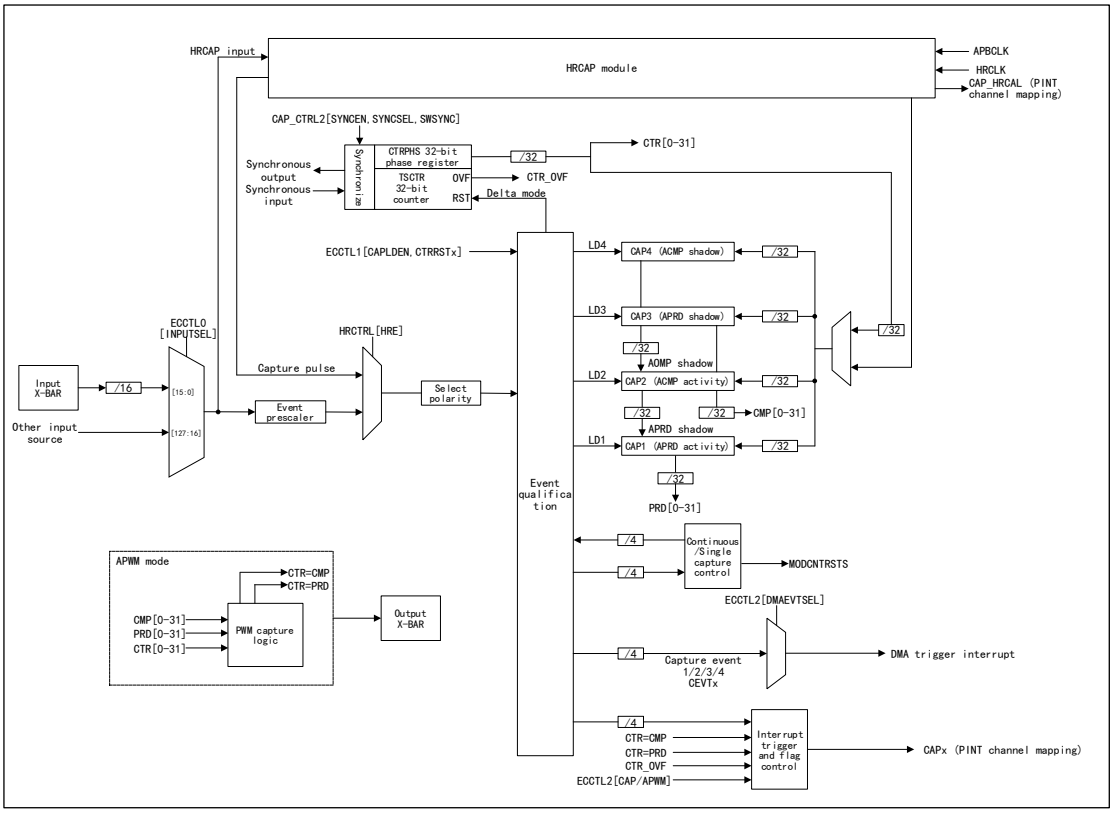
(14) Function description of APWM mode:

- Two 32-bit digital comparators can be used to compare the timestamp counter buses
- Capture register 1/2 can be used as a cycle and comparison value in APWM mode (when capture register 1/2 is not used in CAP mode)
- Double buffering is implemented using capture register 3/4 (APRD and ACMP shadow registers), and the contents can be transmitted to capture register 1/2 when the counter is triggered or immediately transmitted to capture register 1/2 when written.
- During initialization, write two period active registers, compare them, and automatically copy the initial value to the shadow value. The shadow registers can be used for subsequent comparison and updating in operation process.
- Instant mode: In APWM mode, when writing to the active registers (capture register 1/2), the same value will also be written to the shadow register (capture register 3/4). Write to the capture register 3/4 and call the shadow mode

(15) Interrupt event:

- CTR=PRD
- CTR=CMP
- CEVTx (x=1...4)
- CTROVF

Figure 56 CAP Structure Block Diagram



Note: HRCAP submodules are not available on all CAP modules; in such case, the high-resolution multiplexer and hardware are not executed.

5.10.1.2. Electrical data and timing of CAP

Table 103 CAP Timing Requirements

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$tw_{(CAP)}$	Collect input pulse width	Asynchronous	$2tc_{(SCO)}$			ns
		Synchronize	$2tc_{(SCO)}$			
		With the input qualifier	$1t_{c(SCO)}+ t_{w\_(QSW)}$			

Table 104 CAP Switch Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
$t_{w(APWM)}$	Pulse duration, high/low level of APWMx output	20			ns

Notes: Supplementary instructions for use of interrupts: Due to the interrupt handling characteristics of the CPU used by G32R5xx, it is not recommended to use the system-level Clear Pending statement in CAP and HRCAP interrupt programs. If this statement is used, it may be impossible to enter the interrupt again during the program execution in high-frequency capture. If it is not used, there will be no such problem.

5.10.2. High-resolution capture (HRCAP6-HRCAP7)

According to the CAP structure block diagram, the HRCAP submodule is part of Type 1 CAP. The high-resolution capture (HRCAP) module has higher accuracy in measuring external pulse width than the CAP module. HRCAP supports the following functions:

- Measure and scan the distance or sonar
- Measure the voltage on the isolation boundary
- Measure the flow rate
- Measure the instantaneous speed and instantaneous frequency
- Measure the HR period and duty cycle of the pulse sequence period
- Capacitive touch application

5.10.2.1. Main characteristics

(1) Absolute mode pulse width capture

(2) Capture the pulse width in non-high resolution or high-resolution mode

(3) Capture mode:
- Continuous mode
- Single mode

(4) Hardware calibration logic (used for precise high-resolution capture)

(5) In continuous mode, the pulse width capture results support four-level cache

(6) Interrupt is generated on the rising or falling edge

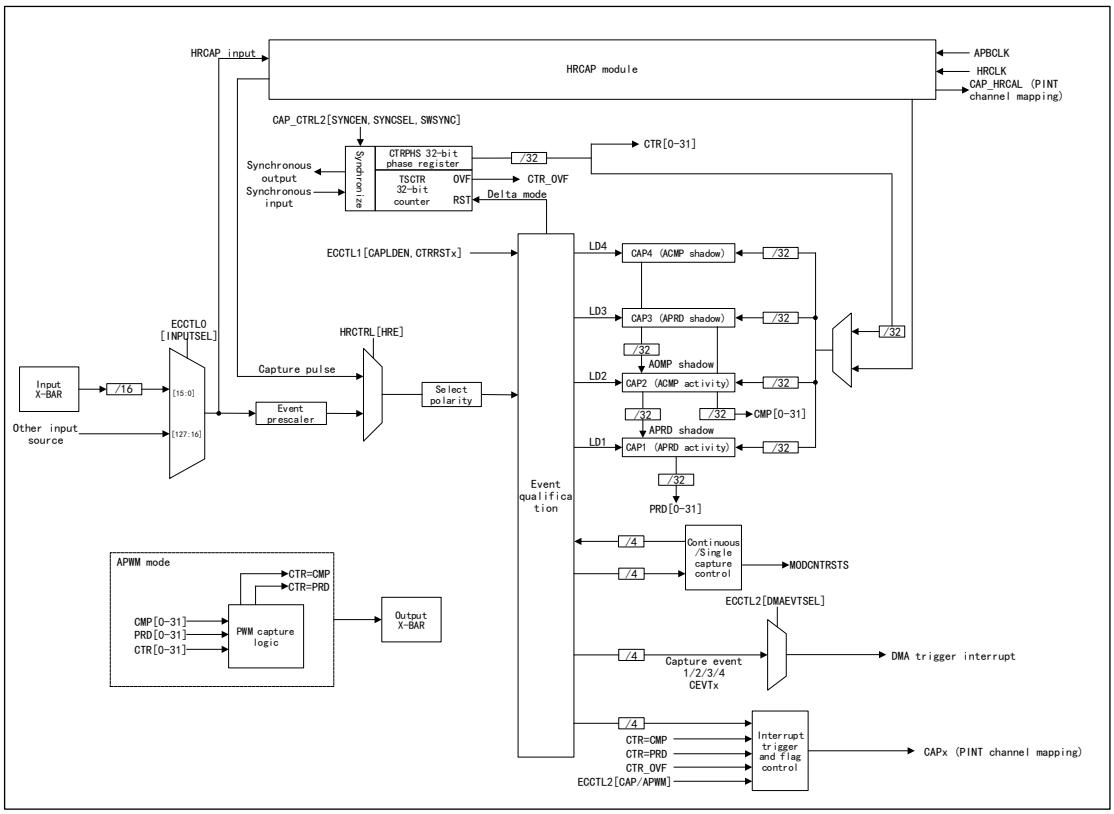
(7) Calibration (offline execution is not required)

(8) Improvement of Type 0 HRCAP:
- The usage of HRCAP is consistent with CAP
  - HRCAP enhancement function is added in CAP6/7, and it allows signals to be asynchronously captured to APBCLK. If the HRCAP enhancement function is used, all CAP hardware can be accessed, but the input qualification or event filters cannot be used due to the synchronization with APBCLK. Each HRCAP submodule also includes a capture channel (in addition to the hardware calibration block).
- The HRCAP enhancement function can be used to access all CAP hard blocks
- The integers and decimals are packaged into 32 bits to reduce software overhead for calculating decimals
- Simplify the calibration scheme
  - HRCAP is always valid
  - Always execute calibration in the background without the need for offline execution of calibation
  - The software costs for calibration is reduced

(9) Each HRCAP channel has the following functions:
- Dedicated calibration interrupt
- HR calibration logic

- All hardware of corresponding CAP

Figure 57 HRCAP Structure Block Diagram



Note: HRCAP submodules are not available on all CAP modules; in such case, the high-resolution multiplexer and hardware are not executed.

5.10.2.2. Electrical data and timing of HRCAP

Table 105 HRCAP Switch Characteristics

Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
Input pulse width		110			ns
Accuracy (1) (2) (3) (4)	Measurement duration ≤ 5μs		±390	540	ps
	Measurement duration > 5μs		±450	1450	ps
Standard deviation			Please refer to the diagram of "Standard Deviation Characteristics"		
Resolution			300		ps

Note:

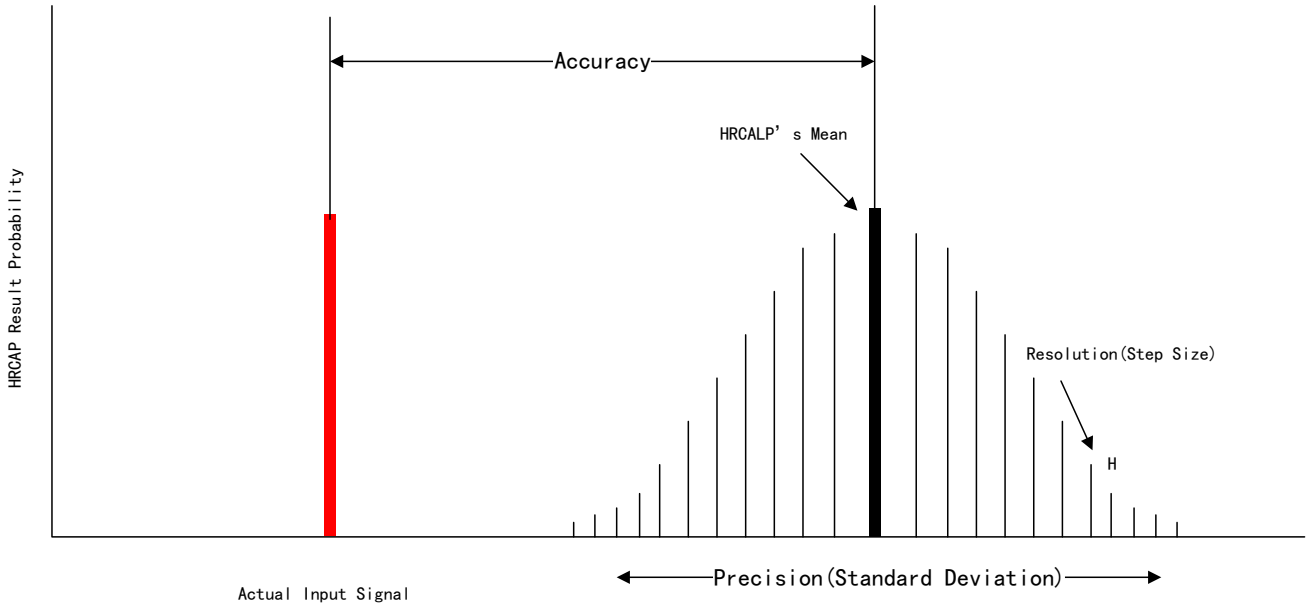
(1) The value obtained using the 100PPM oscillator; the oscillator accuracy directly affects the accuracy of HRCAP.

(2) Use the rising-rising edge or falling-falling edge to complete the measurement.

(3) Due to the difference between VIH and VIL, the edges with opposite polarity will further reduce the accuracy. This impact depends on the slew rate of the signal.

(4) The accuracy is only applicable to measurements that undergo time conversion.

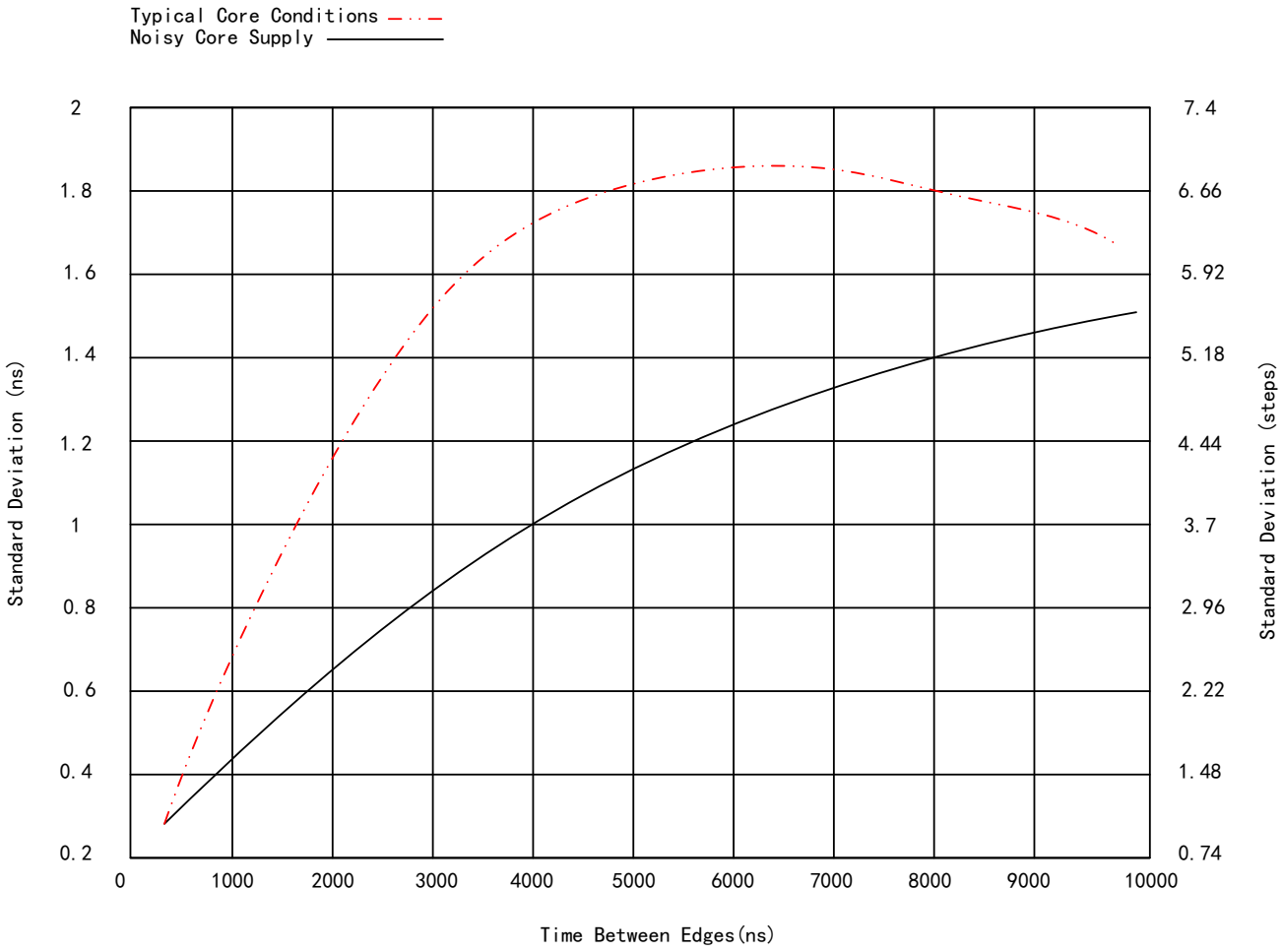
Figure 58 HRCAP Accuracy and Resolution



HRCAP has some changes in performance, and its probability distribution can be described using the following terms:

- Accuracy: The time difference between the input signal and the mean value of HRCAP distribution.
- Accuracy: The width of the HRCAP distribution, given in the form of standard deviation.
- Resolution: Minimum measurable increment.

Figure 59 HRCAP Standard Deviation Characteristics



Note:

(1) Typical core condition: All peripheral clocks are enabled.

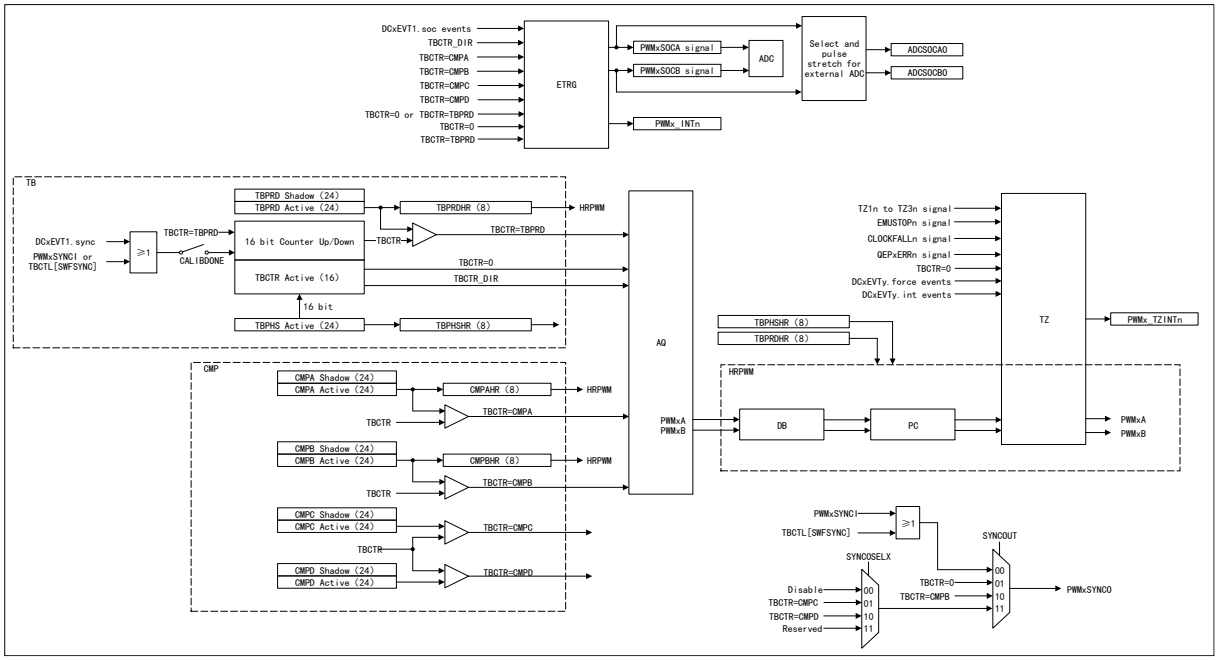
(2) Noisy core power supply: During the measurement period, all core clocks are enabled and disabled at a fixed cycle. This will cause a swing of 18.5mA to the 1.1V power rail during measurement.

(3) Fluctuations in the current and voltage on the 1.1V power rail can cause an increase in the standard deviation of HRCAP. It is important to ensure that the 1.1V power supply is clean, and the internal interference events (e.g. enabling and disabling the clock trees) have been minimized when HRCAP is used.

5.10.3. Pulse width modulator (PWM)

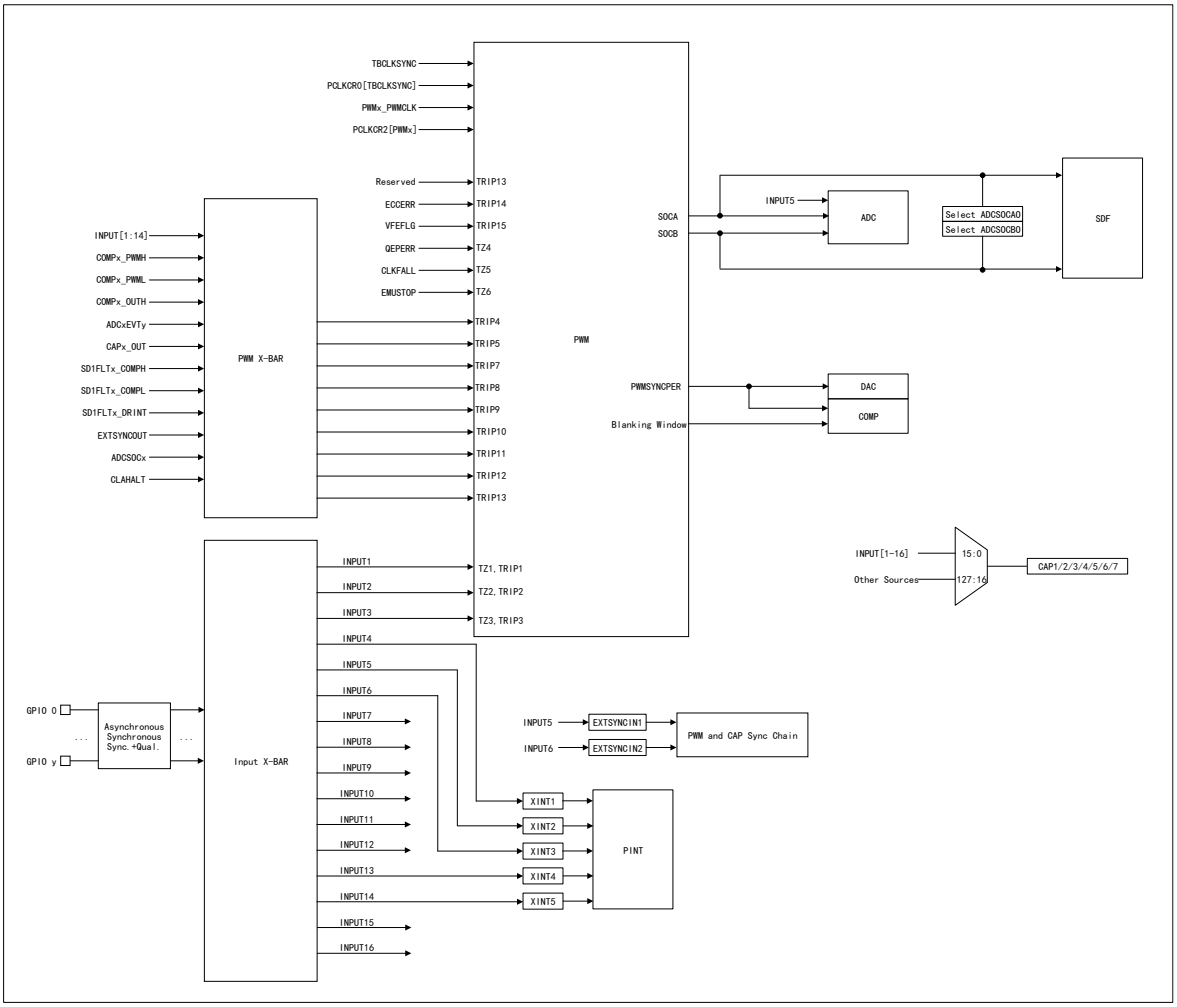
PWM peripherals are key elements for controlling many power electronic systems in commercial and industrial equipment. PWM Class 4 modules generate complex pulse width waveforms with minimal CPU overhead. Some highlights of PWM Class 4 modules include complex waveform generation, dead zone generation, flexible synchronization scheme, advanced jump zone function, and global register overloading function.

Figure 60 Structure Block Diagram for Interconnection between PWM Module and Key Internal Signals



Note: These events are generated by the PWM digital comparison (DC) submodule according to the TRIPIN input level.

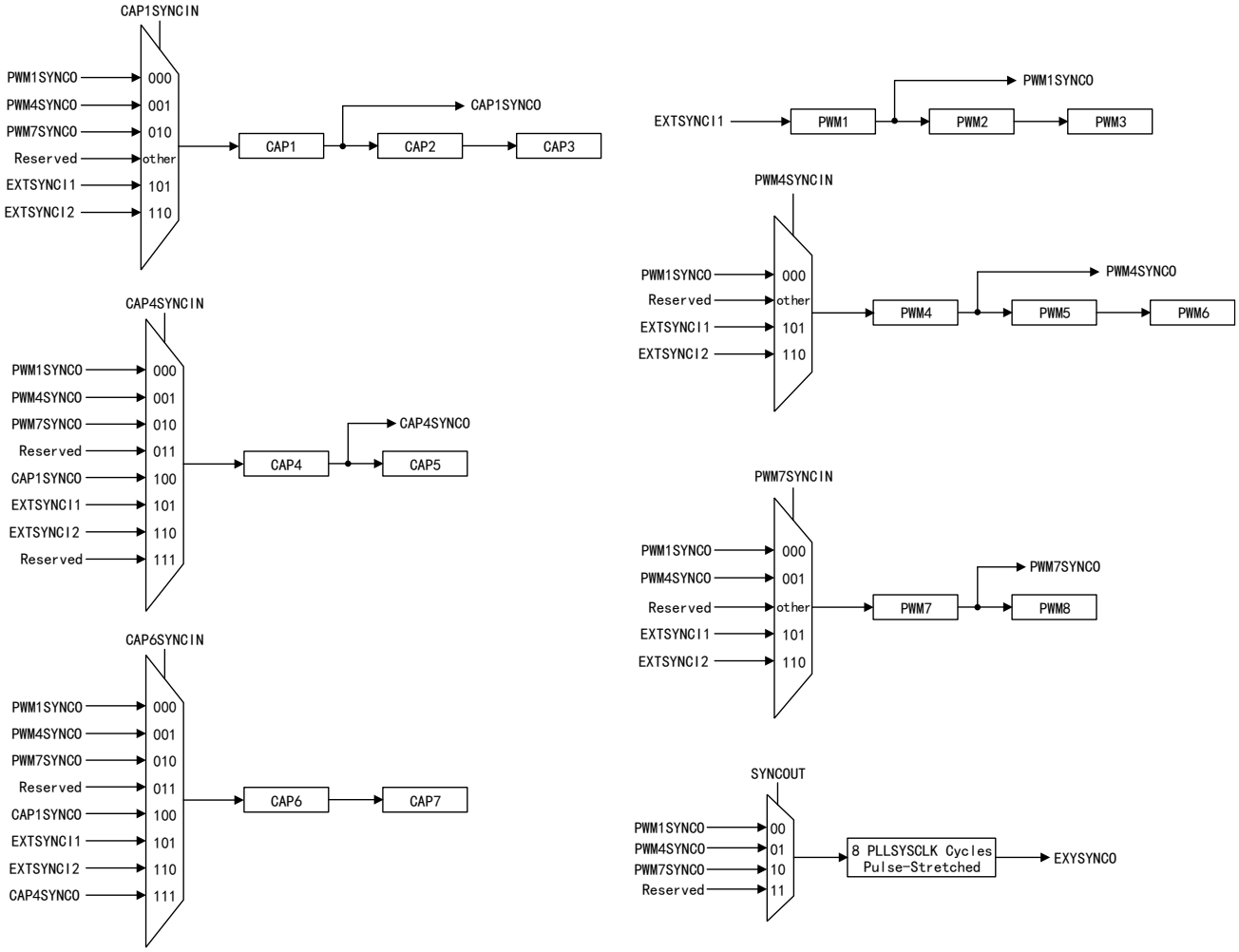
Figure 61 PWM Trip Input Structure Block Diagram



5.10.3.1. Control peripheral synchronization

PWM and CAP synchronization chains allow synchronization between multiple modules of the system.

Figure 62 Structure Block Diagram for Synchronization of Time Base Counters



5.10.3.2. Electrical data and timing of PWM

Table 106 PWM Timing Requirements

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$t_{w(SYNCIN)}$	Synchronous input pulse width	Asynchronous	$2t_{c(PWMCLK)}$	-	Cycle
		Synchronize	$2t_{c(PWMCLK)}$	-	
		With the input qualifier(1)	$1t_{c(PWMCLK)}+ t_{w(IQSW)}$	-	

Note:

(1) For the description of input qualifier parameters, please refer to the table of "General-purpose Input Timing Requirements".

Table 107 PWM Switch Characteristics

Symbol	Parameter	Minimum value	Maximum value	Unit
$t_{w(PWM)}$	Pulse duration, high/low level of PWMx output	20	-	ns
$t_{w(SYNCOUT)}$	Synchronous output pulse width	$4t_{c(APBCLK)}$	-	Cycle
$t_{d(TZ-PWM)}$	Delay time, from jump input activation to forced high level of PWM Delay time, from jump input activation to forced low level of PWM Delay time, from jump input activation to high impedance of PWM	-	35	ns

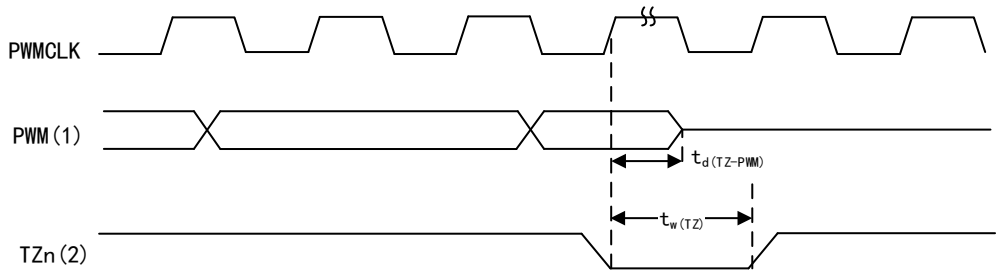
Table 108 Input Timing Requirements for Trip Area

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
tw (TZ)	Pulse duration, low level of TZxn input	Asynchronous	$1t_{c(PWMCLK)}$		Cycle
		Synchronize	$2t_{c(PWMCLK)}$		
		With the input qualifier(1)	$1t_{c(PWMCLK)}+ t_{w(IQSW)}$		

Note:

(1) For the description of input qualifier parameters, please refer to the table of "General-purpose Input Timing Requirements".

Figure 63 PWM Hi-Z Characteristics



Note:

(1) PWM refers to all PWM pins in the device. The state of the PWM pin after TZn is set to a high level depends on the PWM recovery software.

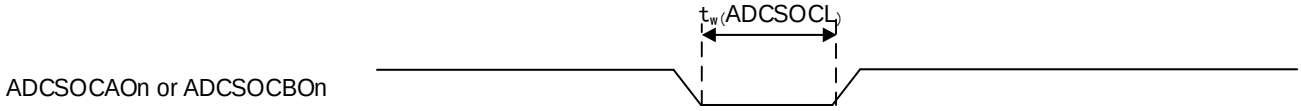
(2) TZn: TZ1n, TZ2n, TZ3n, TRIP1 to TRIP12

5.10.3.3. Electrical data and timing for start of external ADC conversion

Table 109 Switch Characteristics for Start of External ADC Conversion

Symbol	Parameter	Minimum value	Maximum value	Unit
$t_{w(ADCSOCL)}$	Pulse duration, low level of ADCSOCxOn	32tc（APBCLK）		Cycle

Figure 64 ADCSOCAO or ADCSOCBO Timing



5.10.4. High-resolution pulse width modulator (HRPWM)

5.10.4.1. Main characteristics

(1) The minimum allowed HRPWMCLK frequency for HRPWM is 60MHz

(2) It can be used to control the duty cycle and phase of PWM signals

(3) Capable of extending the time resolution

(4) Dead zone high-resolution control
- Allow control of RED and FED during half-cycle clock operation

(5) Allow enabling high-resolution switching for PWM output

(6) High-resolution control of the PWMxB signal output can be enabled by flipping the PWMxA signal output

(7) Applied to the outputs of PWMxA and PWMxB (signal paths A and B of PWM)

(8) Self-check the software mode
- This module is used to check the operation status of HRP logic, that is, check whether it is running as designed

(9) Implement fine edge positioning or time granularity control over PWM signals by extending CMPA, CMPB, and TBPHS registers

(10) Allow high-resolution control over the PWM output signal's high-resolution period, duty cycle, and phase on the devices with PWM modules

5.10.4.2. Electrical data and timing of HRPWM

Table 110 High-resolution PWM Characteristics

Parameter	Minimum value	Typical value	Maximum value	Unit
Micro-edge positioning (HRP) step size (1)		150	310	ps

Note: Applications using the HRPWM characteristics should use the HRP scale factor optimizer (SFO) to estimate software functions.

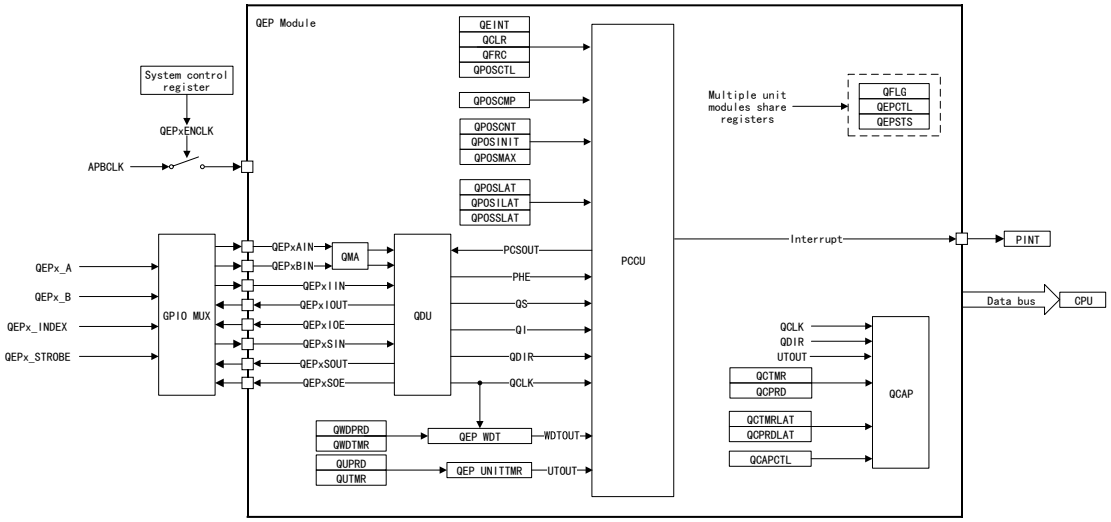
(1) The HRP step size reaches its maximum value at high temperature and the minimum value of the voltage on VDD. The HRP step size will increase with the increase of temperature and reduction of voltage, and decrease with the decrease of temperature and rise of voltage.

5.10.5. Quadrature encoder pulse (QEP)

The QEP peripherals include the following main functional units:
- Programmable input authentication for each pin (part of GPIO MUX)

- Quadrature decoder unit (QDU)
- Position counter and control unit (PCCU) for position measurement
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base (UTIME) for speed/frequency measurement
- Watchdog timer (QWDOG) for detecting stall
- Quadrature mode adapter (QMA)

Figure 65 QEP Structure Block Diagram



5.10.5.1. Electrical data and timing of QEP

Table 111 QEP Timing Requirements

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$t_{w(QEPP)}$	QEP input cycle	Asynchronous [2]/Synchronous	$2t_{c(APBCLK)}$		Cycle
		With the input qualifier[1]	$2[1t_{c(APBCLK)}+ t_{w(IQSW)}]$		
$t_{w(INDEXH)}$	High-level time of QEP index input	Asynchronous [2]/Synchronous	$2t_{c(APBCLK)}$		Cycle
		With the input qualifier[1]	$2t_{c\ (APBCLK)}+ t_{w\ (IQSW)}$		
$t_{w(INDEXL)}$	Low-level time of QEP index input	Asynchronous [2]/Synchronous	$2t_{c(APBCLK)}$		Cycle
		With the input qualifier[1]	$2t_{c\ (APBCLK)}+ t_{w\ (IQSW)}$		
$t_{w(STROBH)}$	High-level time of QEP gating	Asynchronous [2]/Synchronous	$2t_{c(APBCLK)}$		Cycle
		With the input qualifier[1]	$2t_{c\ (APBCLK)}+ t_{w\ (IQSW)}$		
$t_{w(STROBL)}$	Low-level time of QEP gating input	Asynchronous [2]/Synchronous	$2t_{c(APBCLK)}$		Cycle

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
		With the input qualifier(1)	$2t_{c\ (APBCLK)}+ t_{w\ (IQSW)}$		

Note:

(1) For the description of input qualifier parameters, please refer to the table of "General-purpose Input Timing Requirements".

(2) For the restrictions in asynchronous mode, please refer to the table of "Device Errata".

Table 112 QEP Switch Characteristics

Symbol	Parameter	Minimum value	Maximum value	Unit
$t_{d(CNTR)xin}$	Delay time, increment from external clock to counter		$5t_{c(APBCLK)}$	Cycle
$t_{d(PCS-OUT)QEP}$	Delay time, from QEP input edge to synchronous output of position comparison		$7t_{c(APBCLK)}$	Cycle

5.10.6. Σ-Δ filter module (SDF)

SDF is an advanced digital filter designed for motor control systems, which has four independent input channels. In motor control applications, these input channels are usually used for current measurement and resolver position decoding, and each input channel can independently receive the bit streams from the Sigma Delta modulator. It is equipped with four programmable digital demodulation filters. These filters can be precisely adjusted to meet various signal processing requirements. Besides, SDF is equipped with a fast comparator as a secondary filter, which can quickly perform digital threshold comparison for real-time monitoring of overcurrent and undercurrent, and zero-crossing detection of signals.

5.10.6.1. Main characteristics

(1) SDF has four independently configurable main filter (data filter) units:
- The filter module can be enabled or disabled;
- Four types of filter options are provided, including Sinc1, Sinc2, SincFast and Sinc3;
- The oversampling rate (OSR, DOSR) of the data filtering unit is set between 1 and 256;
- Four independent filters can be synchronized through the main filter enable bit or PWM signal;

(2) The SDF module contains four independently configurable secondary filter (comparator) units:
- Able to perform cross detection of high values, low values, and thresholds;
- Four types of filter options are provided, including Sinc1, Sinc2, SincFast and Sinc3;
- The oversampling rate (OSR, DOSR) of the comparator filter unit is set between 1 and 32;

(3) The SDF module has 8 external pins, including four data input pins and four clock input pins:

- The data input pin receives data signals from Sigma-Delta;
- The clock input pin receives clock signals from Sigma-Delta;

(4) PWM signals can also be used to generate the modulator clock required for Sigma-Delta modulator;

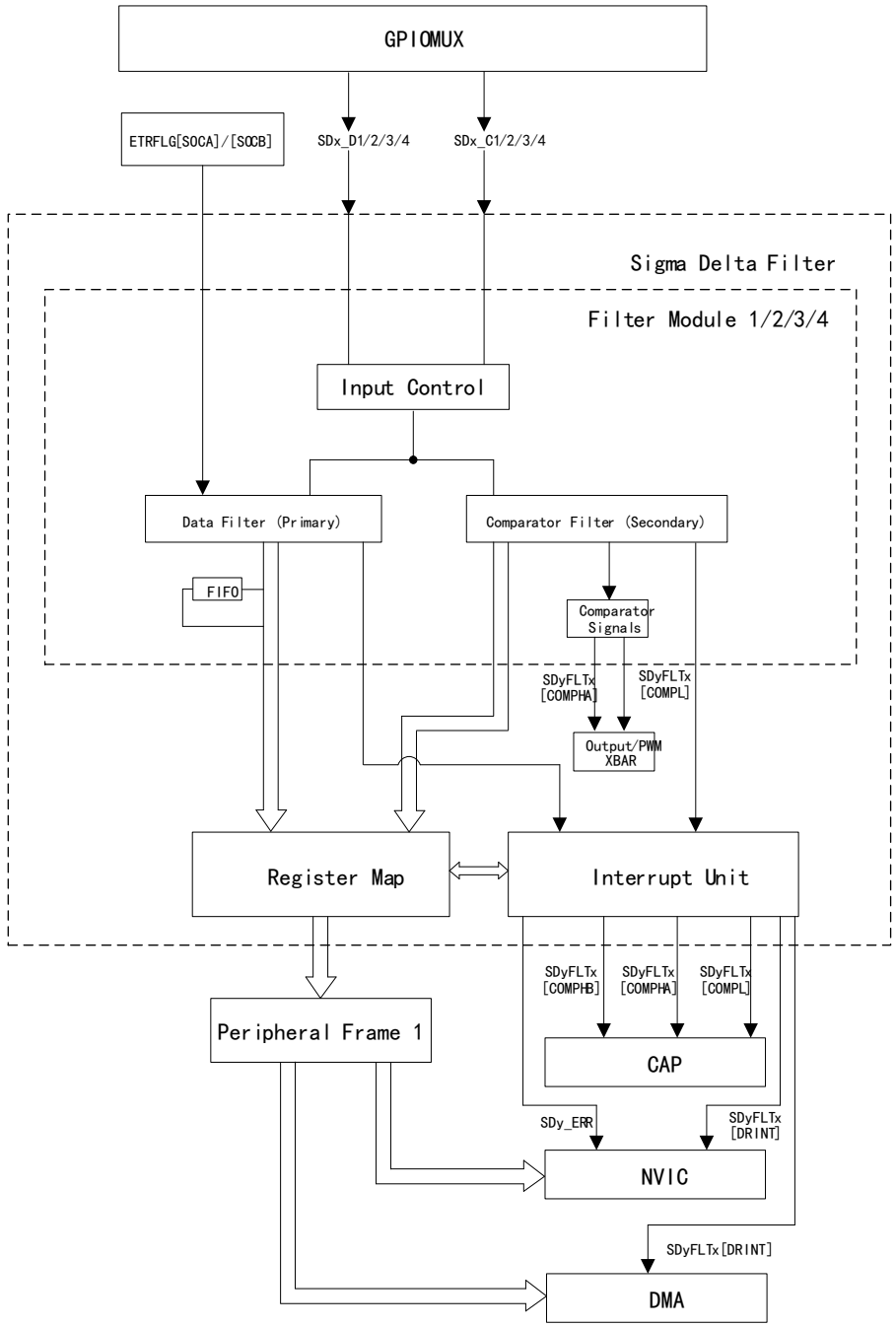
(5) The data filter unit is equipped with a programmable FIFO mode;

(6) SDF allows use ofPWM signals as the source of synchronous data filter channels;

(7) SDF supports different modulator clock operating modes to meet different application requirements:
- Mode 0: The clock frequency of the modulator is the same as the data frequency
- Mode 1: The clock frequency of the modulator is half of the data frequency
- Mode 2: The modulator data adopting Manchester encoding do not need additional clock signals
- Mode 3: The clock frequency of the modulator is twice the data frequency

Note: It is necessary to avoid noise at the SDx_Cy input terminal. To avoid abnormal results of SDF, the minimum pulse width requirement should be met (to avoid noise interference).

Figure 66 SDF Structure Block Diagram



5.10.6.2. Electrical data and timing of SDF

Define SDF operation with asynchronous GPIO by setting GPyQSELn=11.

Table 113 SDF Timing Requirements when Asynchronous GPIO (ASYNC) Options is Used

Symbol	Parameter	Minimum value	Maximum value	Unit
Mode 0				
$t_{c(SDC)M0}$	Cycle time, SDx_Cy	40	256 APBCLK cycles	ns
$t_{W(SDC)M0}$	Pulse duration, SDx_Cy high level	10	$t_{c(SDC)M0}$ – 10	ns

Symbol	Parameter	Minimum value	Maximum value	Unit
$t_{su(SDDV-SDCH)M0}$	Valid set time of SDx_Dy before SDx_Cy becomes high	5		ns
$t_{h(SDCH-SDD)M0}$	Holding time of SDx_Dy waiting after SDx_Cy becomes high	5		ns
Mode 1				
$t_{c(SDC)M1}$	Cycle time, SDx_Cy	80	256 APBCLK cycles	ns
$t_{W(SDC)M1}$	Pulse duration, SDx_Cy high level	10	$t_{c(SDC)M1-10}$	ns
$t_{su(SDDV-SDCL)M1}$	Valid set time of SDx_Dy before SDx_Cy becomes low	5		ns
$t_{su(SDDV-SDCH)M1}$	Valid set time of SDx_Dy before SDx_Cy becomes high	5		ns
$t_{h(SDCL-SDD)M1}$	Holding time of SDx_Dy waiting after SDx_Cy becomes low	5		ns
$t_{h(SDCH-SDD)M1}$	Holding time of SDx_Dy waiting after SDx_Cy becomes high	5		ns
Mode 2				
$t_{c(SDD)M2}$	Cycle time, SDx_Dy	8 $t_{c(APBCLK)}$	20 $t_{c(APBCLK)}$	ns
$t_{w(SDDH)M2}$	Pulse duration, SDx_Dy high level	10		ns
$t_{w(SDD\_LONG\_KEEPOUT)M2}$	SDx_Dy long pulse duration retention time, where the long pulse shall not fall within the listed minimum or maximum values. Long pulse is defined as high or low pulse, and it is the full width of Manchester bit clock cycle. For any integer between 8 and 20, this requirement must be met.	$(N * t_{c(APBCLK)})– 0.5$	$(N * t_{c(APBCLK)})+ 0.5$	ns
$t_{w(SDD\_SHORT)M2}$	SDx_Dy short pulse duration for high or low pulses (SDD_SHORT_H or SDD_SHORT_L). Short pulse is defined as high or low pulse, and it is half the width of Manchester bit clock cycle.	$t_{w(SDD\_LONG)}/2 – t_{c(APBCLK)}$	$t_{w(SDD\_LONG)}/2 + t_{c(APBCLK)}$	ns
$t_{w(SDD\_LONG\_DUTY)M2}$	SDx_Dy long pulse change (SDD_LONG_H – SDD_LONG_L)	$– t_{c(APBCLK)}$	$t_{c(APBCLK)}$	ns
$t_{w(SDD\_SHORT\_DUTY)M2}$	SDx_Dy short pulse (SDD_SHORT_H – SDD_SHORT_L)	$– t_{c(APBCLK)}$	$t_{c(APBCLK)}$	ns
Mode 3				
$t_{c(SDC)M3}$	Cycle time, SDx_Cy	40	256 APBCLK cycles	ns
$t_{W(SDC)M3}$	Pulse duration, SDx_Cy high level	10	$t_{c(SDC)M3} - 5$	ns

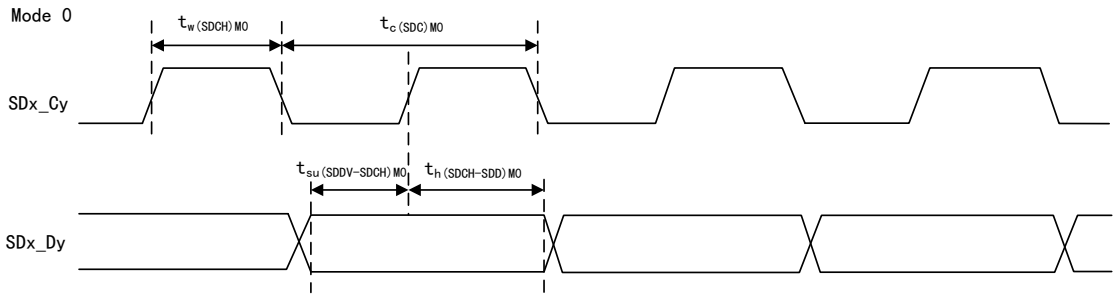
Symbol	Parameter	Minimum value	Maximum value	Unit
$t_{su(SDDV-SDCH)M3}$	Valid set time of SDx_Dy before SDx_Cy becomes high	5		ns
$t_{h(SDCH-SDD)M3}$	Holding time of SDx_Dy waiting after SDx_Cy becomes high	5		ns

5.10.6.2.1. SDF Timing Diagram

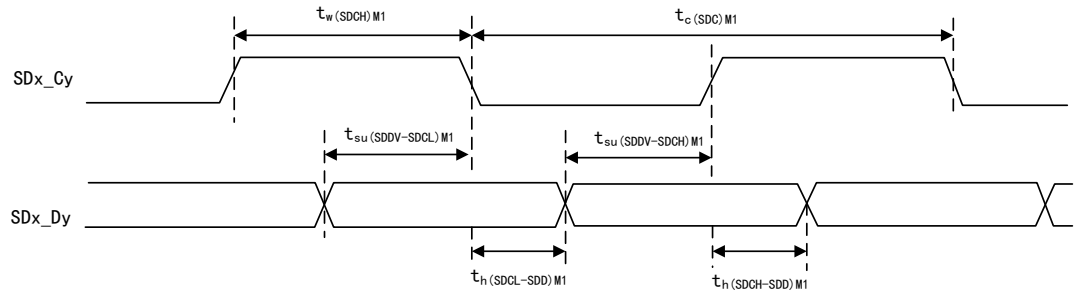
When there is no GPIO input synchronization, the SDF clock input (SDx_Cy pin) directly keeps time for the SDF module. Any interference or ringing noise from these input ends will destroy the operation of the SDF module. Special preventive measures should be taken to cope with these signals so as to ensure clean and noise-free signals that meet the SDF timing requirements. It is recommended to take preventive measures, e.g. applying series termination to the ringing caused by impedance mismatch of the clock driver, and isolating the wiring from other noise signals.

Figure 67 SDF Timing Diagram

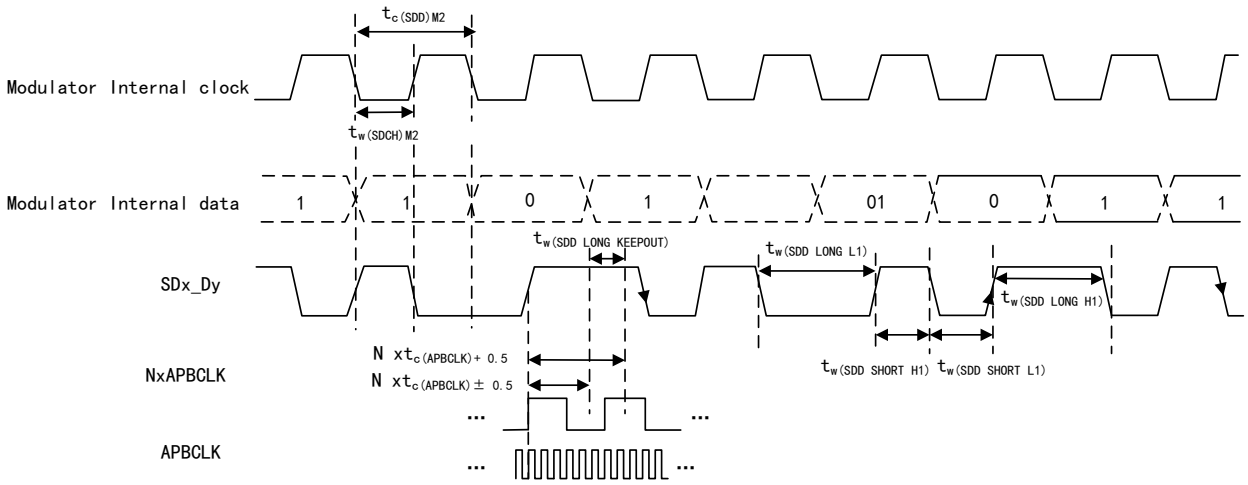
Mode 0



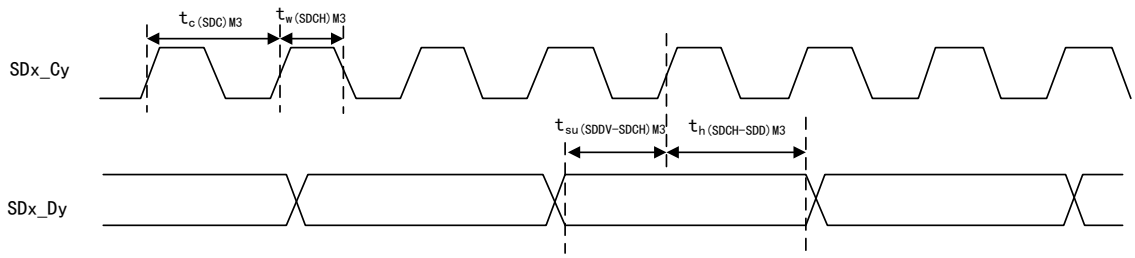
Mode 1



Mode 2(Manchester-encoded-bit stream)



Mode 3 (CLKx is driven externally)



5.10.6.3. Electrical data and timing of SDF (synchronous GPIO)

Define SDF operation with synchronous GPIO by setting GPyQSELn =0. When this synchronous GPIO mode is used, the timing requirement must be met that $t_{w(GPI)}$ pulse duration should be at least 2tc (APBCLK). Configuring SYNC options is crucial for SD-Cx and SD-Dx.

Table 114 SDF Timing Requirements when Synchronous GPIO (SYNC) Options is Used

Symbol	Parameter	Minimum value	Maximum value	Unit
Mode 0				
$t_{c(SDC)M0}$	Cycle time, SDx_Cy	5 APBCLK cycles	256 APBCLK cycles	ns
$t_{W(SDC)M0}$	Pulse duration, SDx_Cy high level	2 APBCLK cycles	3 APBCLK cycles	ns
$t_{su(SDDV-SDCH)M0}$	Valid set time of SDx_Dy before SDx_Cy becomes high	2 APBCLK cycles		ns
$t_{h(SDCH-SDD)M0}$	Holding time of SDx_Dy waiting after SDx_Cy becomes high	2 APBCLK cycles		ns
Mode 1				
$t_{c(SDC)M1}$	Cycle time, SDx_Cy	10 APBCLK cycles	256 APBCLK cycles	ns
$t_{W(SDC)M1}$	Pulse duration, SDx_Cy high level	2 APBCLK cycles	8 APBCLK cycles	ns
$t_{su(SDDV-SDCL)M1}$	Valid set time of SDx_Dy before SDx_Cy becomes low	2 APBCLK cycles		ns
$t_{su(SDDV-SDCH)M1}$	Valid set time of SDx_Dy before SDx_Cy becomes high	2 APBCLK cycles		ns
$t_{h(SDCL-SDD)M1}$	Holding time of SDx_Dy waiting after SDx_Cy becomes low	2 APBCLK cycles		ns
$t_{h(SDCH-SDD)M1}$	Holding time of SDx_Dy waiting after SDx_Cy becomes high	2 APBCLK cycles		ns
Mode 3				
$t_{c(SDC)M3}$	Cycle time, SDx_Cy	5 APBCLK cycles	256 APBCLK cycles	ns
$t_{W(SDC)M3}$	Pulse duration, SDx_Cy high level	2 APBCLK cycles	3 APBCLK cycles	ns
$t_{su(SDDV-SDCH)M3}$	Valid set time of SDx_Dy before SDx_Cy becomes high	2 APBCLK cycles		ns
$t_{h(SDCH-SDD)M3}$	Holding time of SDx_Dy waiting after SDx_Cy becomes high	2 APBCLK cycles		ns

The SDF synchronous GPIO (SYNC) option can protect the SDF module from the damage due to occasional random noise interference on the SDx_Cy pin. These pin interferences may cause error comparator trips and filter outputs. The SDF synchronous GPIO (SYNC) mode does not provide protection when the above timing requirements are violated continuously. Timing violation will damage the data that is directly proportional to the number of data bits that violate the requirements.

5.11. Communication peripherals

5.11.1. Controller area network (CAN)

5.11.1.1. Main characteristics

(1) The maximum bit rate of communication is 1Mbps

(2) Comply with ISO11898-1 Protocol Specifications (CAN protocol 2.0A and 2.0B)

(3) Two interrupt lines: CANINT0 and CANINT1

(4) Support DMA function

(5) Support multiple clock sources

(6) Support software module reset

(7) Support message RAM parity check mechanism

(8) Support suspension mode for debugging operation

(9) Support programmable loopback mode for self-check operation

(10) After entering the Bus-off state, the 32-bit programmable timer will automatically return to bus-on

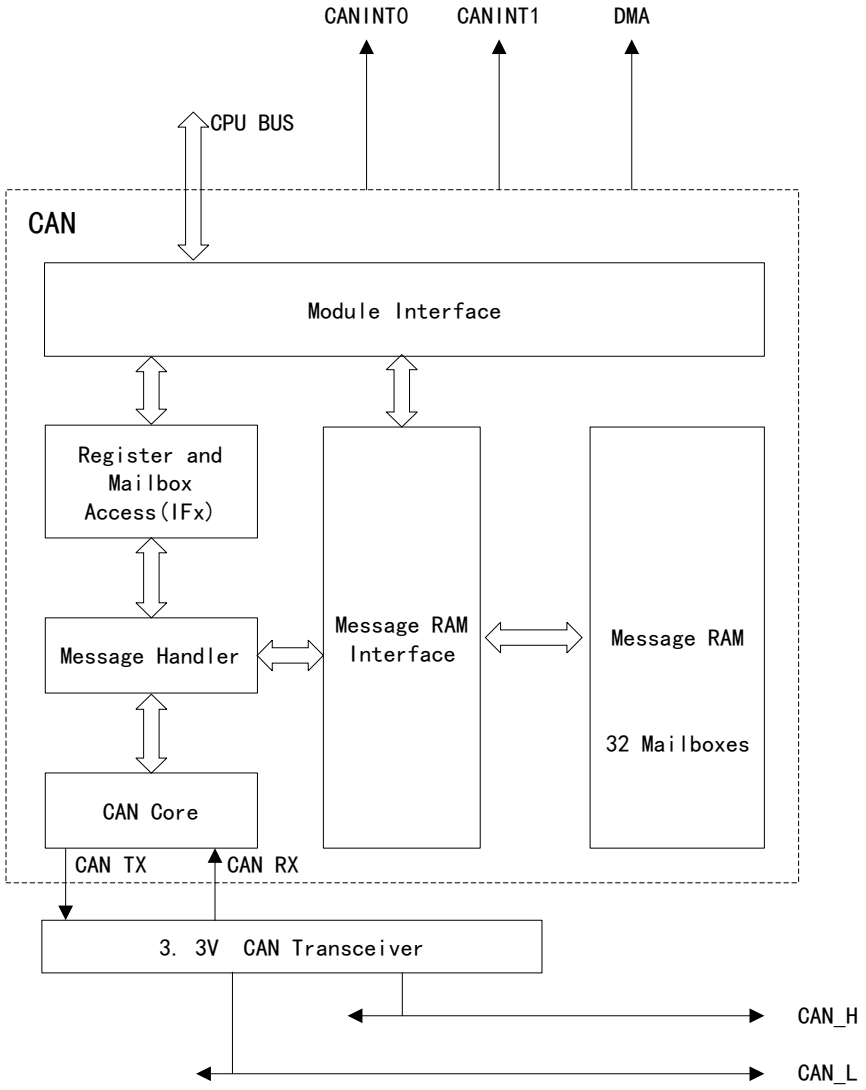
(11) 32 emails, with each having the following characteristics:

- Support transmitting or receiving function
- Support two types of frames: data frame and remote frame
- Support 11-bit standard identifiers or 29-bit extended identifiers, and the identifier receiving masks are configurable
- Able to accommodate data of 0-8 bytes
- Support data RAM and parity configuration
- Each email has an independent identifier mask
- Support programmable FIFO mode

Note:

(1) According to the timing settings used, the accuracy of the on-chip built-in crystal oscillator might not meet the requirements of the CAN protocol. In such case, an external clock source must be used. For details about the accuracy of the on-chip built-in crystal oscillators, please refer to the *Datasheet*.

Figure 68 CAN Structure Block Diagram



5.11.2. Internal integrated circuit (I2C)

5.11.2.1. Main characteristics

(1) Master mode or slave mode can be selected
- Multi-master transmitting and slave receiving
- Multi-slave transmitting and master receiving
- Master transmitting/receiving and receiving/transmitting modes

(2) Free data format mode

(3) 8-bit format transmission

(4) 7-bit and 10-bit addressing mode

(5) Broadcast communication

(6) Start byte mode

(7) Data transmission rate: 10 kbps~400 kbps

(8) Receive FIFO and transmit FIFO

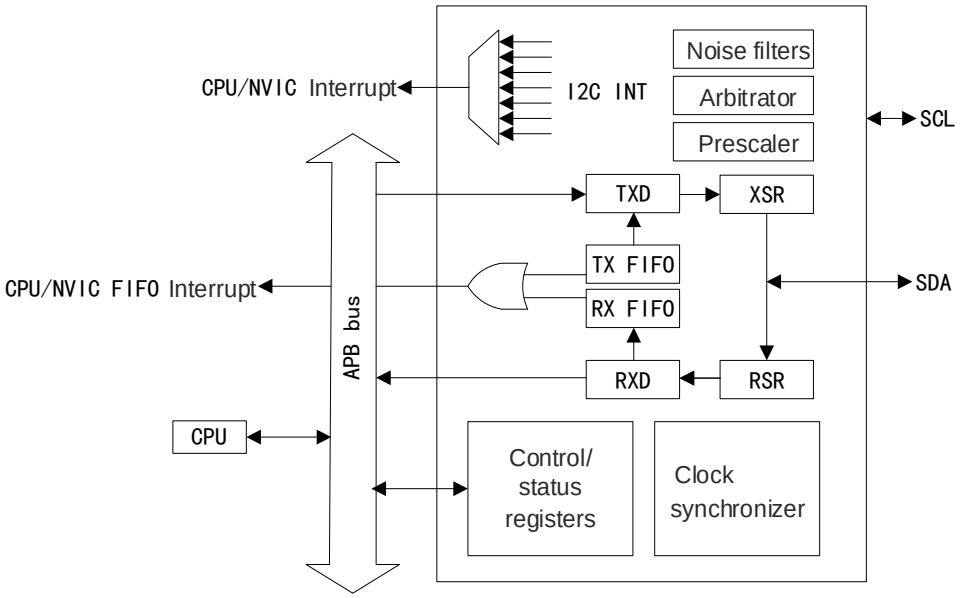
(9) I2C interrupt

- Ready to transmit data
- Ready to receive data
- Register access ready
- Addressed as a slave
- No answer received
- Bus arbitration fails
- Stop condition is detected

(10) I2CFIFO interrupt

- Transmit FIFO interrupt
- Receive FIFO interrupt

Figure 69 I2C Structure Block Diagram



5.11.2.2. Electrical data and timing of I2C

Table 115 I2CTiming Requirements

No.	Symbol	Parameter	Standard mode		Fast mode		Unit
			Minimum value	Maximum value	Minimum value	Maximum value	
T0	f_{mod}	I2C module frequency	7	12	7	12	MHz
T1	$t_{h(SDA-SCL)START}$	Holding time, start condition, delay in SCL fall after SDA falls	4.0		0.6		μs
T2	$t_{su(SCL-SDA)START}$	Set time, repeated start, SCL rise before delay in SDA fall	4.0		0.6		μs
T3	$t_{h(SCL-DAT)}$	Holding time, data after SCL falls	0		0		μs

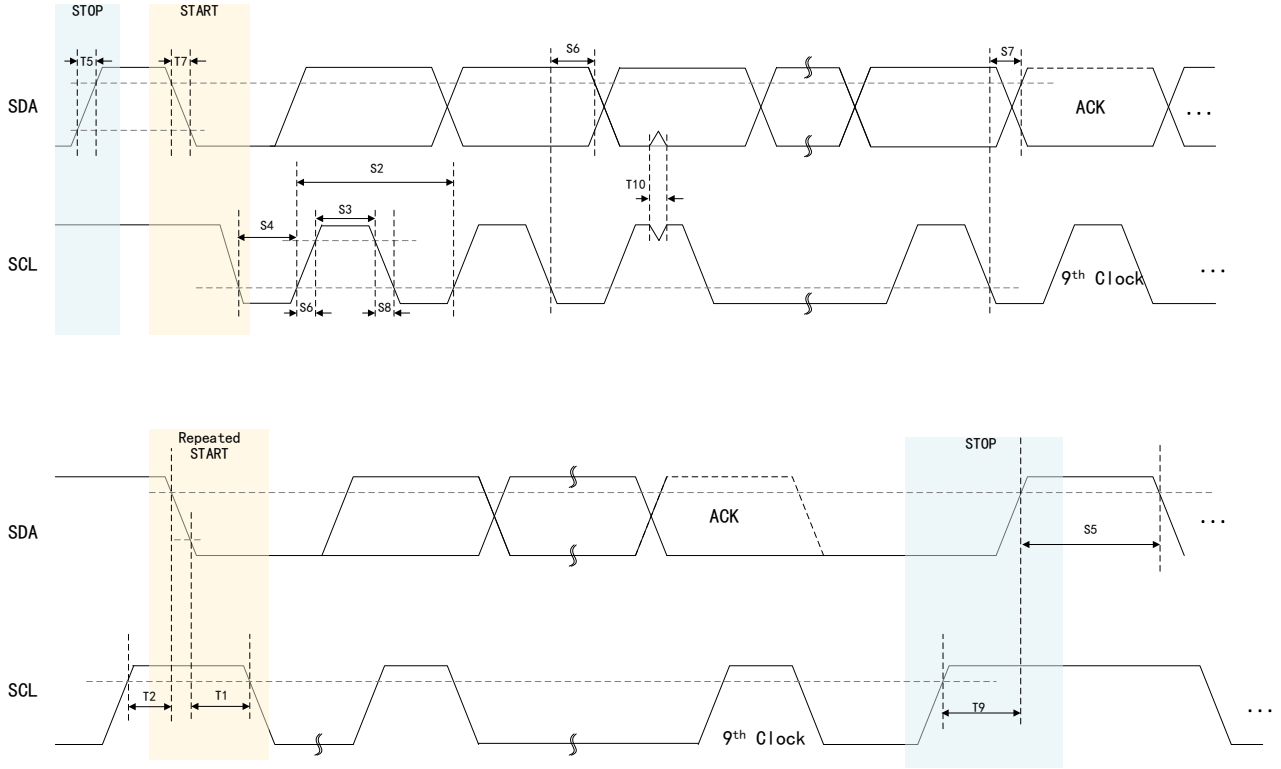
No.	Symbol	Parameter	Standard mode		Fast mode		Unit
			Minimum value	Maximum value	Minimum value	Maximum value	
T4	$t_{su(DAT-SCL)}$	Set time, data before SCL rises	250		100		ns
T5	$tr_{(SDA)}$	Rise time, SDA		1000	20	300	ns
T6	$tr_{(SCL)}$	Rise time, SCL		1000	20	300	ns
T7	$t_{f(SDA)}$	Fall time, SDA		300	11.4	300	ns
T8	$t_{f(SCL)}$	Fall time, SCL		300	11.4	300	ns
T9	$t_{su(SCL-SDA)STOP}$	Set time, stop condition, SCL rise before delay in SDA rise	4.0		0.6		μs
T10	$t_{w(SP)}$	Duration of spike pulses suppressed by the filter	0	50	0	50	ns
T11	C_b	Capacitive load on each bus		400		400	pF

Table 116 I2C Switch Characteristics

No.	Symbol	Parameter	Test conditions	Standard mode		Fast mode		Unit
				Minimum value	Maximum value	Minimum value	Maximum value	
S1	f_{SCL}	SCL clock frequency		0	100	0	400	kHZ
S2	T_{SCL}	SCL clock cycle		10		2.5		μs
S3	$t_{w(SCLL)}$	Pulse duration, low level of SCL clock		4.7		1.3		μs
S4	$t_{w(SCLH)}$	Pulse duration, high level of SCL clock		4.0		0.6		μs
S5	t_{BUF}	Bus idle time between stop and start conditions		4.7		1.3		μs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL falls			3.45		0.9	μs
S7	$t_{v(SCL-ACK)}$	Valid time, confirmation after SCL falls			3.45		0.9	μs
S8	I_I	Input current on the pin	$0.1\ V_{bus} < V_i < 0.9\ V_{bus}$	-10	10	-10	10	μA

In order to meet the requirements of all I2C protocol timing specifications, the I2C module clock (Fmod) must be configured to a value within the range of 7MHz to 12MHz.

Figure 70 I2C Timing Diagram



5.11.3. Power management bus (PMBus) interface

5.11.3.1. Main characteristics

(1) Have PEC function, supporting master-slave mode and I2C mode

(2) There are four signal lines: ALERT, SCL, SDA, and CONTROL

(3) Control the signal level and timing, and resolve addresses and buffer data

(4) Support clock high-level and low-level timeout detection

(5) Have transmit and receive buffers, with a length of up to four bytes

(6) Support two different communication speeds, including standard mode (up to 100kHz) and fast mode (up to 400kHz)

(7) Can handle multiple types of messages in master-slave mode

(8) Can be configured to manually or automatically confirm the device address and command bytes

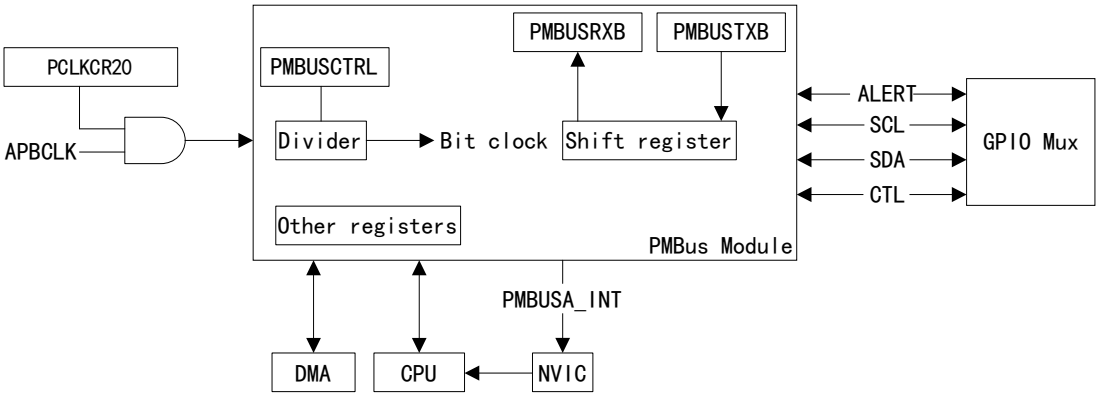
(9) Send EOM interrupt at the end of message transmission

(10) Conditions for triggering a maskable interrupt:

- Low/high timeout of clock
- Bus idle
- The transmit buffer is empty

- Alarm input assertion
- Received data ready/slave address
- Send EOM interrupt

Figure 71 PMBus Module Structure Block Diagram



5.11.3.2. Electrical data and timing of PMBus

Table 117 Electrical Characteristics of PMBus

Symbol	Parameter	Test conditions	Minimum value	Typical value	Maximum value	Unit
VIL	Valid low-level input voltage				0.8	V
V_{IH}	Valid high-level input voltage		2.1		VDDIO	V
V_{OL}	Low-level output voltage	When I_{pullup} = 4mA			0.4	V
I_{OL}	Low-level output current	$V_{OL} \leq 0.4V$	4			mA
t_{SP}	Peak pulse width that must be suppressed by the input filter		0		50	ns
I_i	Input leakage current on each pin	0.1Vbus < Vi < 0.9Vbus	-10		10	μA
C_i	Capacitance on each pin				10	pF

Table 118 Switch Characteristics of PMBus

Symbol	Parameter	Test conditions	Standard mode			Fast mode			Unit
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
f_{SCL}	SCL clock frequency		10		100	10		400	kHZ
t_{BUF}	Bus idle time between stop and start conditions		4.7			1.3			μs
$t_{HD;STA}$	Holding time for		4			0.6			μs

Symbol	Parameter	Test conditions	Standard mode			Fast mode			Unit
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
	start condition - delay from SDA fall to SCL fall								
$t_{SU;STA}$	Set time for repeated start - delay from SCL rise to SDA fall		4.7			0.6			μs
$t_{SU;STO}$	Set time for stop condition - delay from SCL rise to SDA rise		4			0.6			μs
$t_{HD;DAT}$	Data holding time after SCL fall		300			300			ns
$t_{SU;DAT}$	Data set time before SCL rise		250			100			ns
$t_{Timeout}$	Low timeout of clock		25		35	25		35	ms
t_{LOW}	Low-level cycle of SCL clock		4.7			1.3			μs
t_{HIGH}	High-level cycle of SCL clock		4		50	0.6		50	μs
$t_{LOW;SEXT}$	Accumulated clock low-level extension time (slave)	From start to stop			25			25	ms
$t_{LOW;MEXT}$	Accumulated clock low-level extension time (master)	In each byte			10			10	ms
t_r	Rise time of SDA and SCL	From 5% to 95%			1000	365		422	ns
t_f	Fall time of SDA and SCL	From 95% to 5%			300	16		300	ns

5.11.4. Serial communication interface (UART)

USART is a serial communication device that can flexibly exchange full-duplex and half-duplex data with external devices, and meets the requirements of external devices for industry standard NRZ asynchronous serial data format. UART also provides a wide range of baud rate and supports multiprocessor communication. All registers in this module are 8-bit registers. When the register is accessed, the register data

is located in the low byte (bits 7-0), and the high byte (bits 15-8) is read as zero. Writing to high bytes is invalid.

5.11.4.1. Main characteristics

(1) Full-duplex asynchronous communication

(2) Single-line half-duplex communication

(3) NRZ standard format

(4) Characteristics of programmable serial port:
- Data bits: 1 to 8 bits
- Parity bit: Even parity check, odd parity check
- Support 1 and 2 stop bits

(5) Can distinguish data and address bits

(6) Double-buffering receiving and transmitting

(7) Independent transmitter and receiver enable bit

(8) Independent interrupt enable bit

(9) The transmitter and receiver operations can be completed through interrupt or roll polling algorithm-based statuses

(10) 16-level transmit/receive FIFO

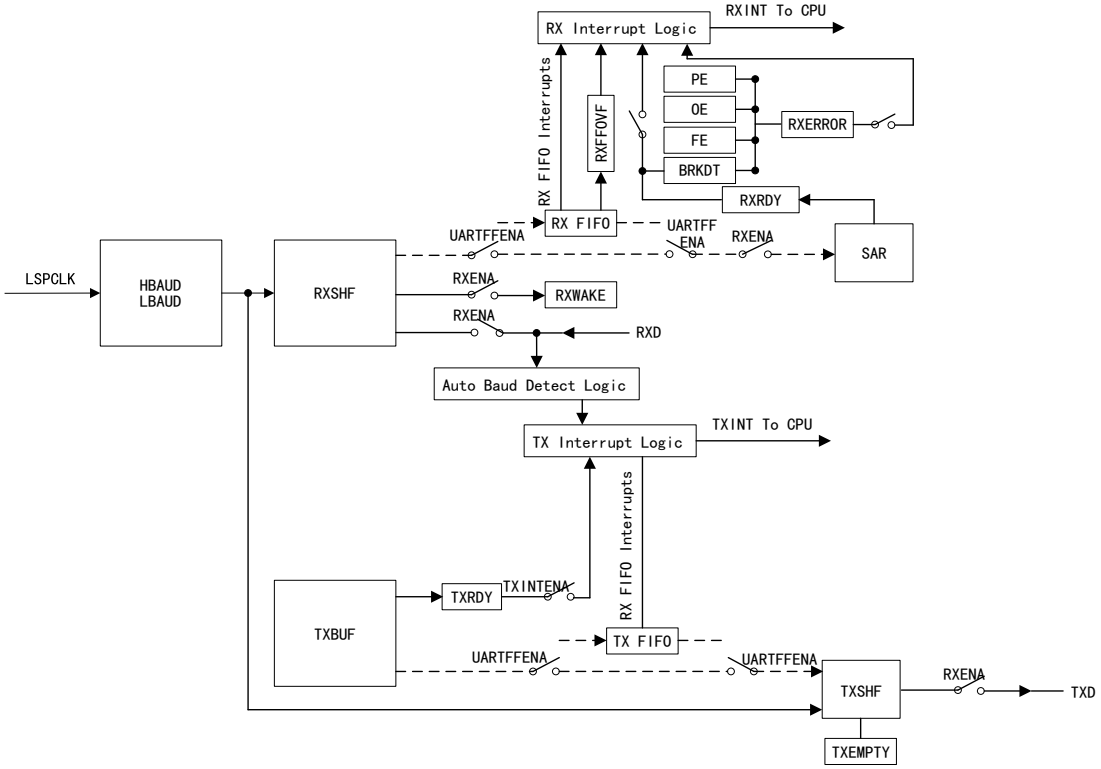
(11) Programmable baud rate generator

(12) Automatic baud rate detection

(13) Multiprocessor communication:
- Idle line mode
- Address bit mode

(14) Status flag bit:
- Transmission detection flag: The transmit register is empty, while the receive register is not empty
- Error detection flag: Overrun error, interrupt detection, parity error, frame error

Figure 72 UART Structure Block Diagram



5.11.5. Serial peripheral interface (SPI)

SPI is a high-speed synchronous serial input/output port, and is used for communication between MCU and peripherals or other controllers, including extending peripherals or external I/O using ADC converters, shift registers, and display drivers. It can work in master or slave mode, supports multi-device communication, and has 125 kinds of programmable transmission baud rates, and the transmitted character length can be set to 1-16 bits. To reduce the CPU usage, it supports 16-level transmit/receive FIFO function.

5.11.5.1. Main characteristics

(1) The polarity and phase of the clock are programmable, and four clock schemes are supported

- No-delay rising edge: Low level of SPICLK is invalid. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
- Delay rising edge: Low level of SPICLK is invalid. SPI transmits data half a cycle in advance on the rising edge of the SPICLK signal, and receives data on the rising edge of the SPICLK signal.
- No-delay falling edge: High level of SPICLK is valid. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Delay falling edge: High level of SPICLK is valid. SPI transmits data half a cycle in advance on the falling edge of the SPICLK signal, and receives data on the falling edge of the SPICLK signal.

(2) 125 kinds of programmable transmission baud rates

(3) Support 1-16-bit transmission data

(4) Support master/slave mode

(5) Support FIFO function, with 16 programmable interrupt levels

(6) Support DMA function

(7) Support transmission delay control

(8) SPI high-speed mode

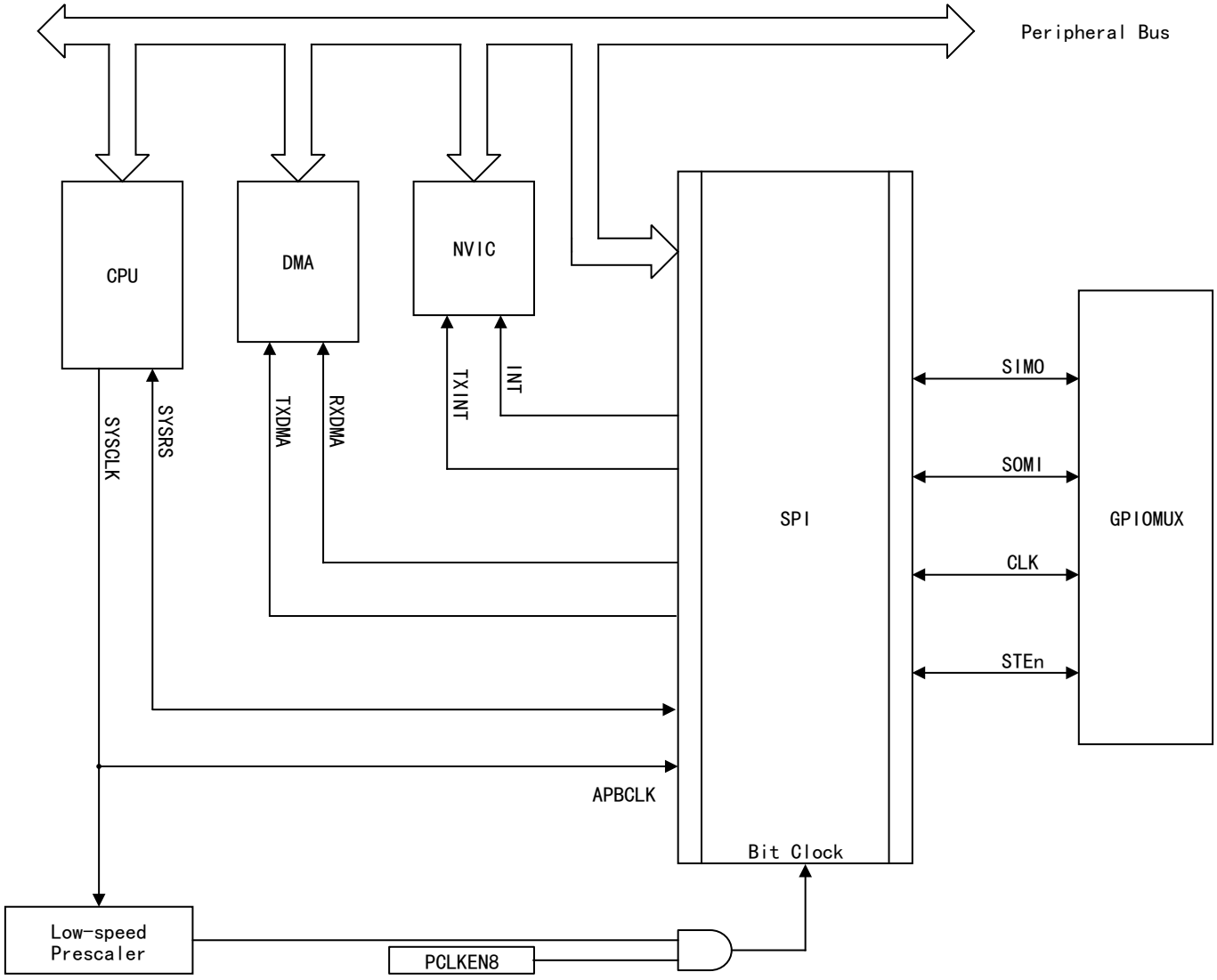
(9) SPI 3-line mode

(10) Support digital audio transmission function

(11) Synchronous transmitting and receiving operations (the transmitting function can be disabled by software)

(12) Complete transmitting and receiving operations through interrupt drive or roll polling algorithm

Figure 73 CPU Interface Structure Block Diagram of SPI



5.11.5.2. Electrical data and timing of SPI

For all timing parameters of SPI high-speed mode, it is assumed that the load capacitance on SPICLK, SPISIMO and SPISOMI is 5pF.

5.11.5.2.1. Timing of non-high speed master mode

Table 119 Switch Characteristics of Non-high-speed Master Mode of SPI

No.	Symbol	Parameter	(BRR+1) condition (1)	Clock phase=0		Clock phase=1		Unit
				Minimum value	Maximum value	Minimum value	Maximum value	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even number	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd number	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{W(SPC1)M}$	Pulse	Even	$0.5t_{c(SPC)M}$ - 3	$0.5t_{c(SPC)M}$ + 3	$0.5t_{c(SPC)M}$ - 3	$0.5t_{c(SPC)M}$ + 3	

No.	Symbol	Parameter	(BRR+1) condition (1)	Clock phase=0		Clock phase=1		Unit
				Minimum value	Maximum value	Minimum value	Maximum value	
		duration, SPICLK, the first pulse	number					ns
			Odd number	$0.5t_{c(SPC)M}+0.5t_{c(LSPCLK)}-3$	$0.5t_{c(SPC)M}+0.5t_{c(LSPCLK)}+3$	$0.5t_{c(SPC)M}-0.5t_{c(LSPCLK)}-3$	$0.5t_{c(SPC)M}-0.5t_{c(LSPCLK)}+3$	
3	$t_{W(SPC2)M}$	Pulse duration, SPICLK, the second pulse	Even number	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M+3}$	$0.5t_{c(SPC)M}-3$	$0.5t_{c(SPC)M}+3$	ns
			Odd number	$0.5t_{c(SPC)M}-0.5t_{c(LSPCLK)}-3$	$0.5t_{c(SPC)M}-0.5t_{c(LSPCLK)}+3$	$0.5t_{c(SPC)M}+0.5tc(LSPCLK)-3$	$0.5t_{c(SPC)M}+0.5t_{c(LSPCLK)}+3$	
4	$t_{d(SIMO)M}$	Delay time, the time from SPICLK to SPISIMO becoming valid	Even number		5	$0.5t_{c(SPC)M}-4$		ns
			Odd number		5	$0.5t_{c(SPC)M}+0.5t_{c(SPCLK)}-1$		
5	$t_{v(SIMO)M}$	Valid time, the time of SPISIMO becoming valid after SPICLK	Even number	$0.5t_{c(SPC)M}-6$		$0.5t_{c(SPC)M}-6$		ns
			Odd number	$0.5t_{c(SPC)M}-0.5t_{c(LSPCLK)}-3$		$0.5t_{c(SPC)M}-0.5t_{c(LSPCLK)}-1$		
23	$t_{d(SPC)M}$	Delay time, the time from SPISTEn becoming valid to SPICLK	Even number, odd number	$1.5t_{c(SPC)M}-3t_{c(APBCLK)}-3$		$2t_{c(SPC)M}-3t_{c(APBCLK)}-3$		ns
24	$t_{d(STE)M}$	Delay time, the time from SPICLK to SPISIMO becoming invalid	Even number	$0.5t_{c(SPC)M}-6$		$0.5t_{c(SPC)M}-6$		ns
			Odd number	$0.5t_{c(SPC)M}-0.5t_{c(LSPCLK)}-3$		$0.5t_{c(SPC)M}-0.5t_{c(LSPCLK)}-1$		

Note:

(1) When (SPIBRR + 1) is an even number or SPIBRR is 0 or 2, the (BRR + 1) condition is an even number. When (SPIBRR + 1) an odd number and SPIBRR is greater than 3, the (BRR + 1) condition is an odd number.

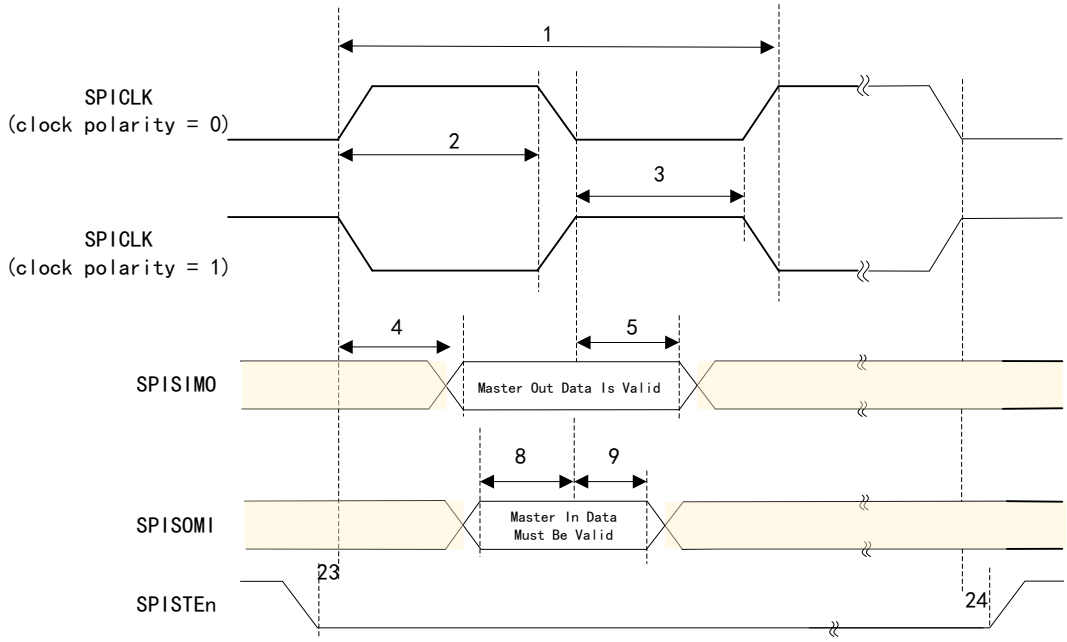
Table 120 Timing Requirements for Non-high-speed Master Mode of SPI

No.	Symbol	Parameter	(BRR+1) condition (1)	Minimum value	Maximum value	Unit
8	$t_{su(SOMI)M}$	Set time of SPISOMI becoming valid before SPICLK	Even number, odd number	20		ns
9	$t_{h(SOMI)M}$	Holding time of SPISOMI becoming valid after SPICLK	Even number, odd number	0		ns

Note:

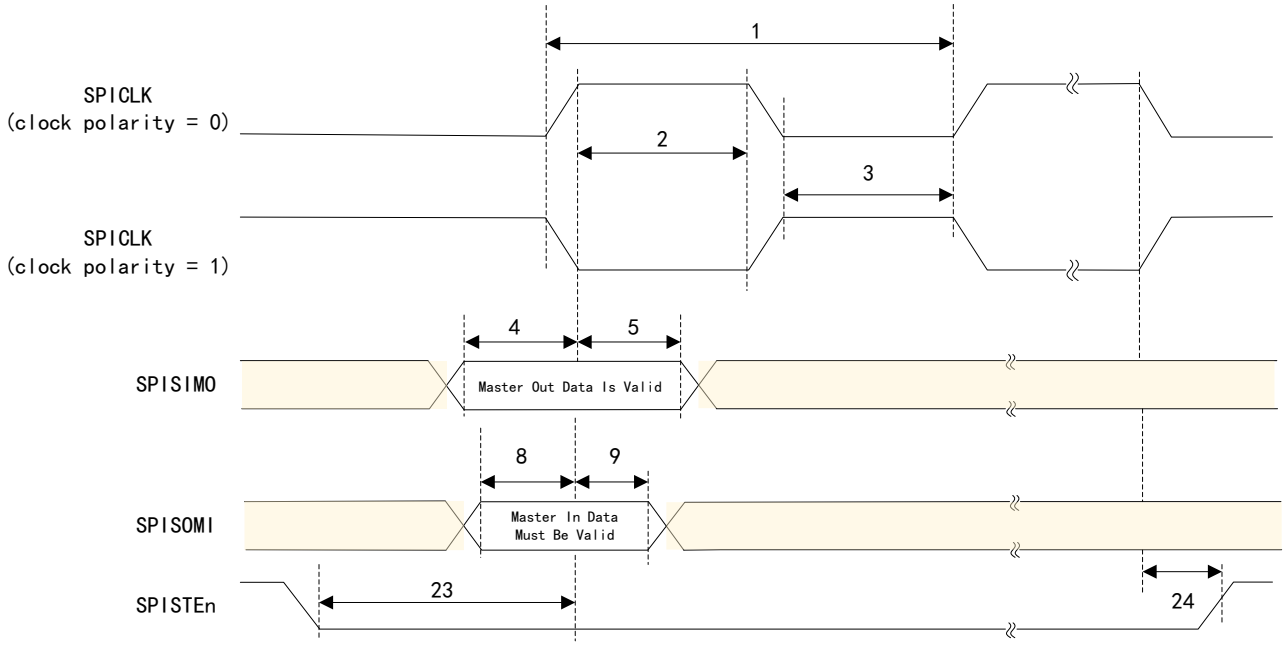
(1) When (SPIBRR + 1) is an even number or SPIBRR is 0 or 2, the (BRR + 1) condition is an even number. When (SPIBRR + 1) an odd number and SPIBRR is greater than 3, the (BRR + 1) condition is an odd number.

Figure 74 External Timing of Non-high-speed SPI Master Mode (Clock Phase = 0)



Note: In addition to the situation of back-to-back transmission of words in FIFO and non-FIFO modes, SPISTEn will be become a stop state at the tail end of the words.

Figure 75 External Timing of Non-high-speed SPI Master Mode (Clock Phase = 1)



Note: In addition to the situation of back-to-back transmission of words in FIFO and non-FIFO modes, SPISTEn will be become a stop state at the tail end of the words.

Figure 7-85. External timing of SPI master mode (clock phase=1)

5.11.5.2.2. Timing of non-high-speed slave mode

Table 121 Switch Characteristics of Non-high-speed Slave Mode of SPI

No.	Symbol	Parameter	Minimum value	Maximum value	Unit
15	$t_{d(SOMI)S}$	Delay time, the time from SPICLK to SPISOMI becoming valid		16	ns
16	$t_{v(SOMI)S}$	Valid time, the time of SPISOMI becoming valid after SPICLK	0		ns

Table 122 Timing Requirements for Non-high-speed Slave Mode of SPI

No.	Symbol	Parameter	Minimum value	Maximum value	Unit
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_c$（SYSCLK）		ns
13	$t_{W(SPC1)S}$	Pulse duration, SPICLK, the first pulse	$2t_{c(SYSCLK)}$–1		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK, the second pulse	$2t_{c(SYSCLK)}$–1		ns
19	$t_{su(SIMO)S}$	Set time of SPISIMO becoming valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
20	$t_{h(SIMO)S}$	Holding time of SPISIMO becoming valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Set time of SPISTE becoming valid before SPICLK (clock phase=0)	$2t_{c(SYSCLK)}$+ 2		ns
		Set time of SPISTE becoming valid before SPICLK (clock phase=1)	$2t_{c(SYSCLK)}$+ 22		ns

26	$t_{h(STE)S}$	Holding time of SPISTE becoming invalid after SPICLK	$1.5t_{c(SYSCLK)}$		ns

Figure 76 External Timing of Non-high-speed SPI Slave Mode (Clock Phase = 0)

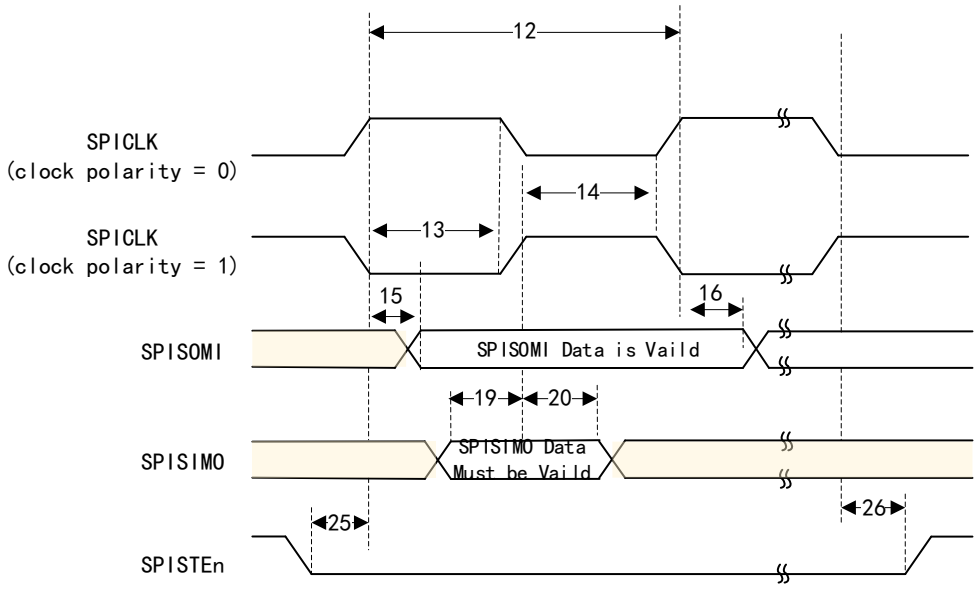
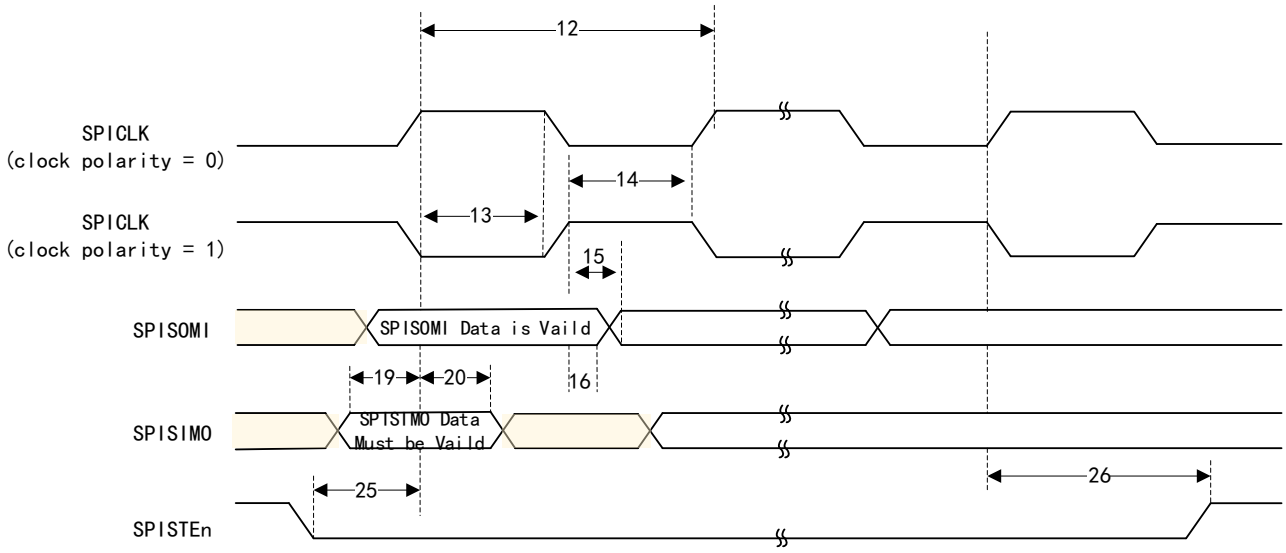


Figure 77 External Timing of Non-high-speed SPI Slave Mode (Clock Phase = 1)



5.11.5.2.3. Timing of high-speed master mode

Table 123 Switch Characteristics of High-speed Master Mode of SPI

No.	Symbol	Parameter	(BRR+1) condition (1)	Clock phase=0		Clock phase=1		Unit
				Minimum value	Maximum value	Minimum value	Maximum value	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even number	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd number	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	

No.	Symbol	Parameter	(BRR+1) condition (1)	Clock phase=0		Clock phase=1		Unit
				Minimum value	Maximum value	Minimum value	Maximum value	
2	$t_{W(SPC1)M}$	Pulse duration, SPICLK, the first pulse	Even number	$0.5t_{c(SPC)M}$ -1	$0.5t_{c(SPC)M}$ +1	$0.5t_{c(SPC)M}$ - 3	$0.5t_{c(SPC)M}$ + 3	ns
			Odd number	$0.5t_{c(SPC)M}$ +0.5tc（(SPCLK)–1	$0.5t_{c(SPC)M}$ +$0.5t_{c(LSPCLK)}$+1	$0.5t_{c(SPC)M}$ - $0.5t_{c(LSPCLK)}$-3	$0.5t_{c(SPC)M}$ - $0.5t_{c(LSPCLK)}$+3	
3	$t_{W(SPC2)M}$	Pulse duration, SPICLK, the second pulse	Even number	$0.5t_{c(SPC)M}$ – 1	$0.5t_{c(SPC)M}$ +1	$0.5t_{c(SPC)M}$-3	$0.5t_{c(SPC)M}$ + 3	ns
			Odd number	$0.5t_{c(SPC)M}$ – $0.5t_{c(LSPCLK)}$– 1	$0.5t_{c(SPC)M}$ – $0.5t_{c(LSPCLK)}$+1	$0.5t_{c(SPC)M}$ +0.5tc(LSPCLK)–3	$0.5t_{c(SPC)M}$ + $0.5t_{c(LSPCLK)}$+3	
4	$t_{d(SIMO)M}$	Delay time, the time from SPICLK to SPISIMO becoming valid	Even number		3	$0.5t_{c(SPC)M}$ - 4		ns
			Odd number		3	$0.5t_{c(SPC)M}$ +$0.5t_{c}$（(SPCLK)–1		
5	$t_{v(SIMO)M}$	Valid time, the time of SPISIMO becoming valid after SPICLK	Even number	$0.5t_{c(SPC)M-4}$		$0.5t_{c(SPC)M}$ - 6		ns
			Odd number	$0.5t_{c(SPC)M}$ - $0.5t_{c(LSPCLK)}$– 1		$0.5t_{c(SPC)M}$ - $0.5t_{c(LSPCLK)}$–1		
23	$t_{d(SPC)M}$	Delay time, the time from SPISTEn becoming valid to SPICLK	Even number, odd number	$1.5t_{c(SPC)M}$ - $3t_{c(APBCLK)}$– 1		$2t_{c(SPC)M}$ - $3t_{c(APBCLK)}$–1		ns
24	$t_{d(STE)M}$	Delay time, the time from SPICLK to SPISIMO becoming invalid	Even number	$0.5t_{c(SPC)M}$ - 4		$0.5t_{c(SPC)M}$ - 6		ns
			Odd number	$0.5t_{c(SPC)M}$ - $0.5t_{c(LSPCLK)}$– 1		$0.5t_{c(SPC)M}$ - $0.5t_{c(LSPCLK)}$–1		

Note:

(1) When (SPIBRR + 1) is an even number or SPIBRR is 0 or 2, the (BRR + 1) condition is an even number. When (SPIBRR + 1) an odd number and SPIBRR is greater than 3, the (BRR + 1) condition is an odd number.

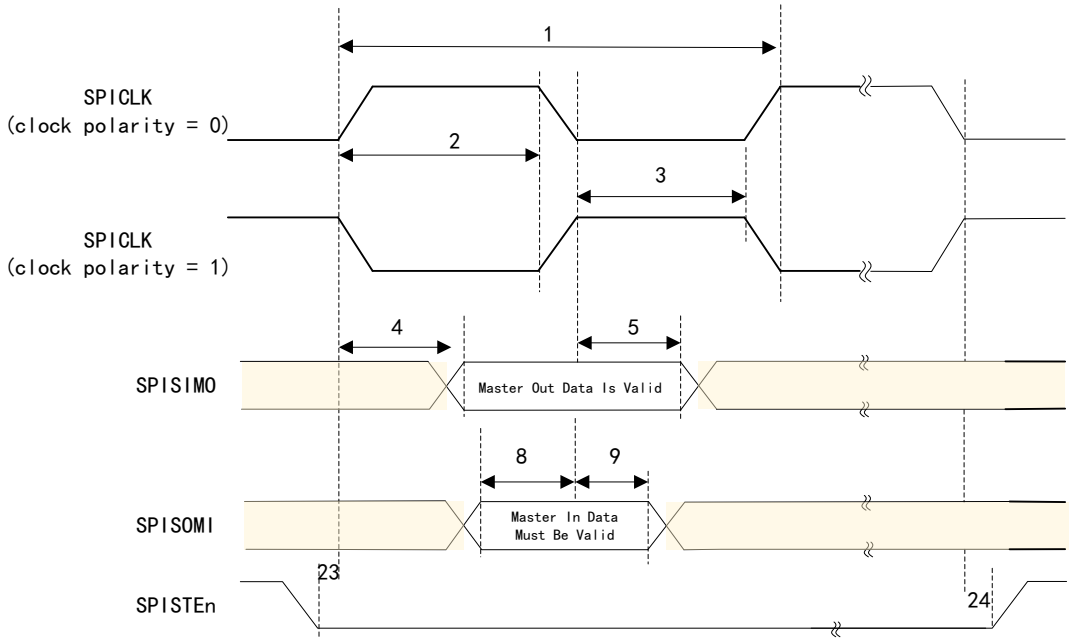
Table 124 Timing Requirements for High-speed Master Mode of SPI

No.	Symbol	Parameter	(BRR+1) condition (1)	Minimum value	Maximum value	Unit
8	$t_{su(SOMI)M}$	Set time of SPISOMI becoming valid before SPICLK	Even number, odd number	2		ns
9	$t_{h(SOMI)M}$	Holding time of SPISOMI becoming valid after SPICLK	Even number, odd number	11		ns

Note:

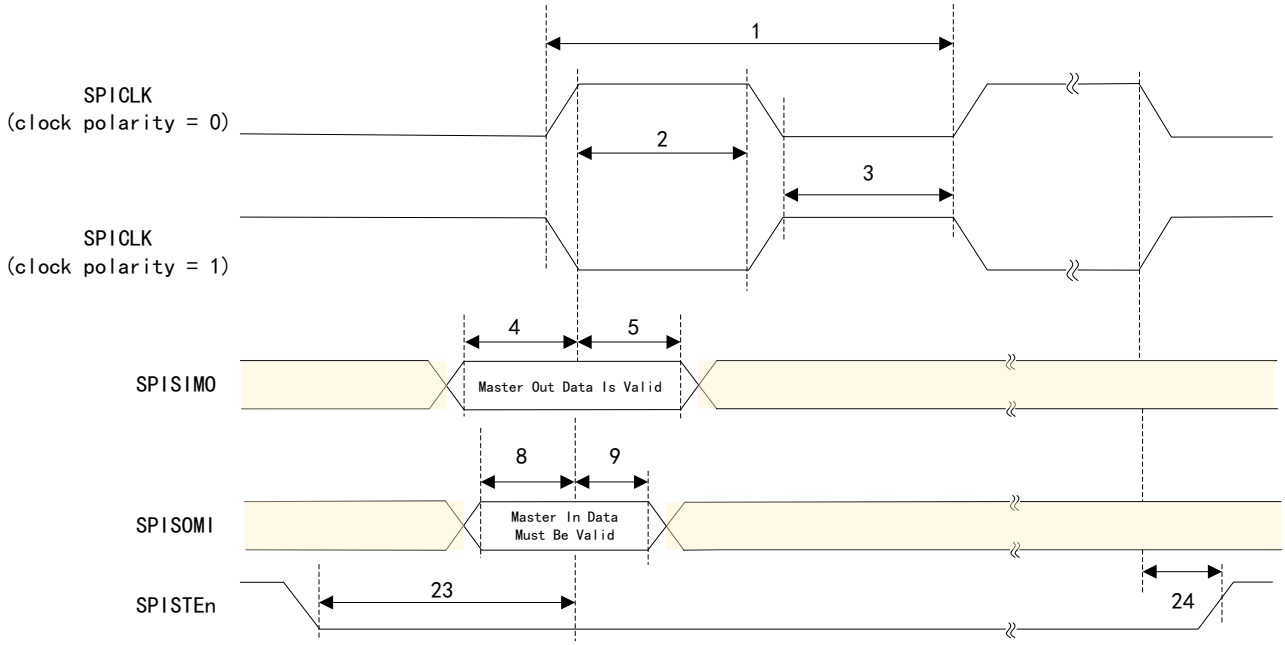
(1) When (SPIBRR + 1) is an even number or SPIBRR is 0 or 2, the (BRR + 1) condition is an even number. When (SPIBRR + 1) an odd number and SPIBRR is greater than 3, the (BRR + 1) condition is an odd number.

Figure 78 External Timing of High-speed SPI Master Mode (Clock Phase = 0)



Note: In addition to the situation of back-to-back transmission of words in FIFO and non-FIFO modes, SPISTE will be become a stop state at the tail end of the words.

Figure 79 External Timing of High-speed SPI Master Mode (Clock Phase = 1)



Note: In addition to the situation of back-to-back transmission of words in FIFO and non-FIFO modes, SPISTE will be become a stop state at the tail end of the words.

5.11.5.2.4. Timing of high-speed slave mode

Table 125 Switch Characteristics of high-speed Slave Mode of SPI

No.	Symbol	Parameter	Minimum value	Maximum value	Unit
15	$t_{d(SOMI)S}$	Delay time, the time from SPICLK to SPISOMI becoming valid		14	ns
16	$t_{v(SOMI)S}$	Valid time, the time of SPISOMI becoming valid after SPICLK	0		ns

Table 126 Timing Requirements for High-speed Slave Mode of SPI

No.	Symbol	Parameter	Minimum value	Maximum value	Unit
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(APBCLK)}$		ns
13	$t_{W(SPC1)S}$	Pulse duration, SPICLK, the first pulse	$2t_{c(APBCLK)}-1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK, the second pulse	$2t_{c(APBCLK)}-1$		ns
19	$t_{su(SIMO)S}$	Set time of SPISIMO becoming valid before SPICLK	$1.5t_{c(APBCLK)}$		ns
20	$t_{h(SIMO)S}$	Holding time of SPISIMO becoming valid after SPICLK	$1.5t_{c(APBCLK)}$		ns
25	$t_{su(STE)S}$	Set time of SPISTE becoming valid before SPICLK	$1.5t_{c(APBCLK)}$		ns
26	$t_{h(STE)S}$	Holding time of SPISTE becoming invalid after SPICLK	$1.5t_{c(APBCLK)}$		ns

Figure 80 External Timing of High-speed SPI Slave Mode (Clock Phase = 0)

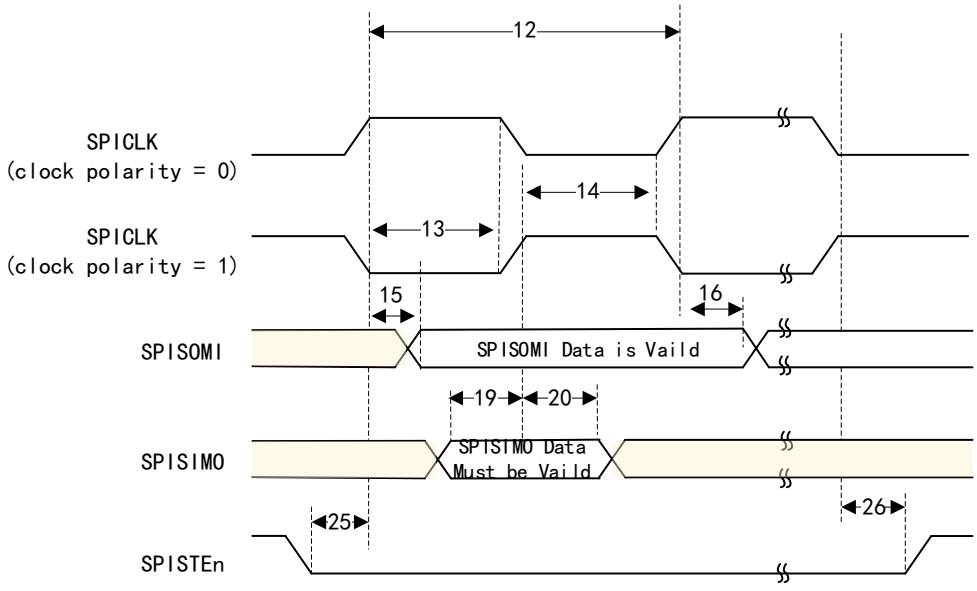
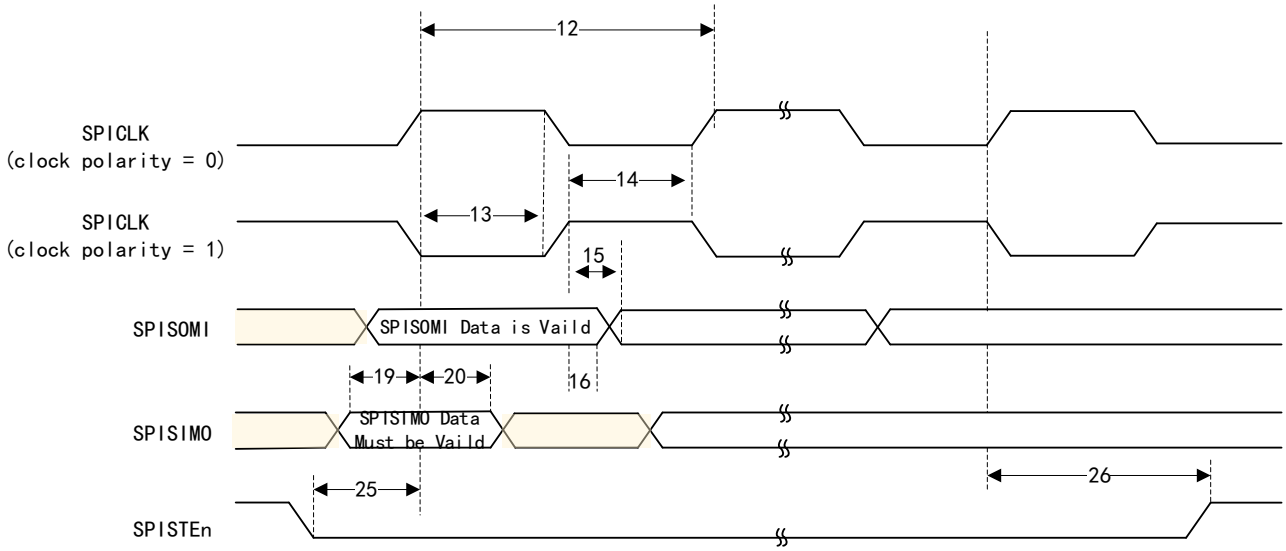


Figure 81 External Timing of High-speed SPI Slave Mode (Clock Phase = 1)



5.11.6. Local interconnection network (LIN)

LIN can be used as a serial communication interface, and in this compatible mode, the LIN function is compatible with other independent serial port modules (UART), but the registers and codes are different. When the module is used as a serial port, it is in compatible mode.

Through configuration, this module can serve as UART or LIN, and the hardware characteristics are enhanced so that G32R501 can be compatible with the LIN function.

The module complies with the LIN2.1 protocol specified in the LIN specification package. The LIN standard is based on the UART serial data link format, and it is used for multicast transmission between network nodes.

5.11.6.1. Main characteristics

(1) Conform to LIN1.3, 2.0, and 2.1 protocols

(1) Multi-buffering receiving and transmitting units

(2) The main header can be automatically generated, including the following fields
- Synchronization field
- Programmable synchronous interrupt field
- Identifier field

(3) Identification mask, used to filter messages

(4) 2 priority encoded interrupt lines, used for receiving and transmitting ID, errors, and statuses

(5) It supports automatic wake-up, and can generate wake-up signals, and configure timeout time

(6) It supports automatic bus idle detection, and LIN2.0 checksum

(7) It supports detection of errors, including:
- Parity check error
- Synchronization field error
- Checksum error
- No-response error
- Bus error
- Bit error

(8) It supports 2^{31} programmable transfer rate (7 decimal places)

(9) The highest baud rate is 20kpbs

(10) It can transmit and receive data through DMA

(11) LINTX and LINRX are used as external pins, and the LINRX master level is awakened by the transceiver

(12) Slave synchronization functions are as follows:
- Synchronous verification

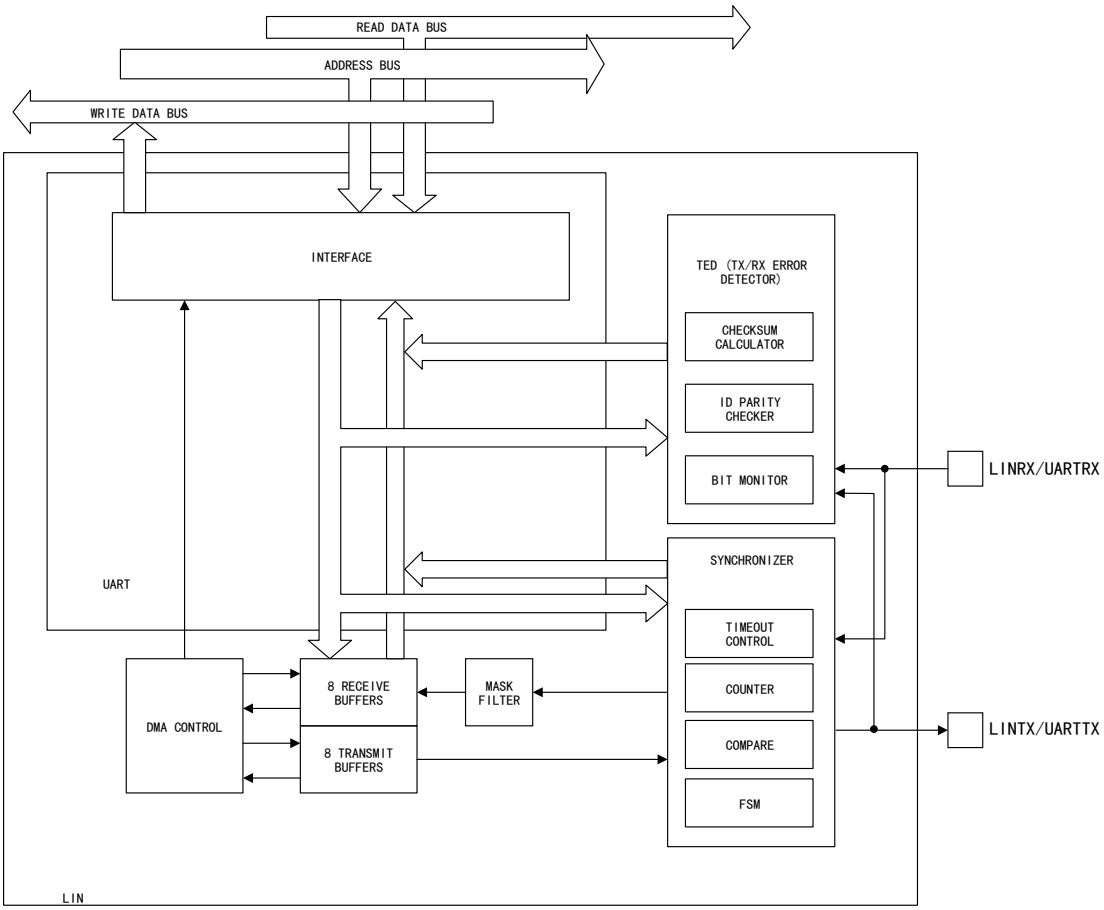
- Synchronous interrupt detection
- Update baud rate (optional)

(13) Update wake-up/sleep

(14) Enhancement options:

- Synchronizer finite state machine (FSM) frames, supporting frame processing
- Processing extended frame
- Baud rate generator

Figure 82 Structure Block Diagram of UART/LIN Block



5.11.7. Quad serial peripheral interface (QSPI)

QSPI is a programmable serial data bus interface, which has four transmission modes: send and receive, send-only, receive-only, and EEPROM read. The transmission mode is controlled by software. QSPI can be configured as a serial host or slave, and the main processor can access the data, control, and status information on QSPI through the AHB interface. In addition, QSPI can be connected to DMA using a set of optional DMA signals.

5.11.7.1. Main characteristics

(1) Integrate AHB interface, conforming to AMBA2.0 specification, with a fixed 32-bit data width

(2) It can be configured as the master or slave mode, and supports communication with other serial master or serial slave peripherals

(3) The serial interface is configurable, and supports multiple serial communication protocols:
- SPI
- SSP
- National Semiconductor Microwire

(4) It supports DMA controller interface, allowing QSPI to connect with DMA controller through handshake interface.

(5) It supports multi-master conflict detection, and can detect access from multiple serial masters on the serial bus and report conflicts to the processor

(6) Programmable delay for sampling time of received serial data bits (rxd) in master mode, so as to achieve higher serial data bit rates

(7) Advanced RXD sampling delay: data sampling at the falling edge of the clock

(8) Programmable characteristics
- Serial interface: It supports multiple serial communication protocols such as SPI, SSP, and National Semiconductor Microwire
- Clock bit rate: Programmable serial baud rate for data transmission
- Clock extension: It supports clock extension in enhanced SPI format
- Data item: The size of data items each time transmitted can be programmed to be 4-32 bits

(9) Configurable characteristics
- FIFO depth: The depth of the transmit and receive FIFO buffers can be configured to 2-256 words, with a fixed FIFO bit width of 32 bits
- Slave device selection output quantity: When QSPI serves as a serial master, it can generate 1-16 serial slave device selection output signals
- Slave device selection control: It can be configured to control the target serial slave devices by dedicated hardware slave device selection line or by software
- The way the interrupt line is led out from QSPI to the interrupt controller can be configured to be led out separately or be led out by combining all interrupt lines into one interrupt line
- Serial clock polarity and phase are configurable
- Data prefetch function can be configured: Prefetch the data of the next continuous operation during the current XIP transaction
- Parallel XIP and non-XIP are configurable: A separate FIFO can be created for XIP data

(10) Enhanced SPI mode
- It supports enhanced/multi-channel (dual/four/eight channel) SPI

- It supports DDR mode, in which read data gating is supported so as to obtain higher frequencies
- Instructions, address length, wait cycle, and data frame size are programmable
- Can be programmed to skip addresses and instruction segments

(11) It supports XIP mode

- The instruction and address length is programmable
- The data frame size is directly mapped from AHB transmission
- It supports transmission of fixed data frame sizes
- It supports continuous transmission mode

(12) It supports data masking

(13) It Supports the Hyperbus protocol

5.11.7.2. Characteristics and Timing of QSPI

Table 127 QSPI Timing Requirements

No.	Symbol	Parameter (1)	Minimum value	Maximum value	Unit
1	f_{SCK}	QSPI clock frequency	0	62.5	MHz
2	t_{su}	Set time of input, for all QSPI IO	2	-	ns
3	t_{HD}	Holding time of input, for all QSPI IO	2	-	ns
4	t_{HO}	Holding time of output, for all QSPI IO	2	8	ns
5	t_V	Time of valid output data	-	8	ns

Note:

(1) The QSPI timing parameters are measured under the operating conditions of a 3.3V power supply and a 10pF output load.

(2) If the user reads external Flash using QSPI at a high clock frequency, the delays that may occur in the transmission path and during sampling can lead to sampling deviations. Therefore, to ensure correct data sampling, QSPI supports data delay sampling functionality. More information can be found in the *QSPI User Manual*.

6. Device characteristics

Table 128 Main Characteristics of Devices

Module	Characteristics	System advantages
Processing performance		
Real-time control CPU	Cortex-M52: 250 MHz Flash: Up to 640 KB RAM: Up to 28 KB 32-bit floating point unit (FPU32) Triangular mathematical unit (TMU) Viterbi, complex math and CRC	The 32-bit Cortex-M52 core provides 250MHz signal processing performance for floating-point or fixed-point arithmetic. **FPU32:** It supports IEEE-754 single-precision and double-precision floating-point arithmetic **TMU:** Use accelerators to accelerate the execution speed of trigonometric functions and arithmetic operations, so as to

Module	Characteristics	System advantages
	unit (VCU)	improve the computation speed of control applications (e.g. PLL and DQ transformations). It helps to achieve faster control loops, increase the efficiency, and optimize the component sizes. Special instructions support non-linear PID control algorithms. **VCU:** Reduce the delay in common complex mathematical operations in encoded applications
Sensing		
Analog-to-digital converter (ADC) (12 bits)	Up to 3 ADC modules 3.45MSPS sampling rate Up to 31 channels	ADC performs precise parallel sampling for all three-phase currents and DC buses, with zero jitter. PPB: The post-processing module reduces the complexity of ADC ISR and shortens the current loop period. Increase in the number of ADC channels: It provides higher effective MSPS (oversampling) and typical ENOB for better control loop performance in multiphase applications.
Comparator subsystem (COMP)	COMP 2 window comparators 2 12-bit DAC DAC slope generation Provide low DAC output on external pins Digital filter 60ns trip detection time Slope compensation	The applications of COMP include: Applicable to such applications as peak current mode control, switch mode power supply, power factor correction, and voltage tripping monitoring. By means of the blanking window and filtering function provided by the analog comparator subsystem, PWM trip triggering and elimination of unnecessary noises can be realized. It provides better control accuracy: PWM can be controlled through comparators and 12-bit DAC (COMP) without further CPU configuration. Implement protection and control using the same pin.
Quadrature encoder pulse (QEP)	2 QEP modules	The applications of QEP include: It can be used for direct connection with linear or rotary incremental encoders, helping to capture the position, direction, and velocity information of rotary machinery in high-performance motion and position control systems. In addition, it can also be used to count input pulses from external devices (e.g. sensors).
Capture(CAP)/ High-resolution capture (HRCAP)	7 CAP modules (2 with HRCAP function); Measure the time elapsed between events (up to 4 events with timestamps); Connect to any GPIO through the input X-BAR; When not used in acquisition mode, the CAP module can be configured as a single-channel PWM output (APWM)	The applications of CAP include: Speed measurement of rotary machinery (e.g. sensing toothed sprockets through Hall sensors) Measurement of duration between pulses of position sensors Measurement of period and duty cycle of pulse sequence signals Decoding of the amplitude of current or voltage from duty cycle encoded current/voltage sensors

Module	Characteristics	System advantages
	2 HRCAP channels Measurement of the width of external pulses with a typical resolution of 300ps	The applications of HRCAP include: High-resolution period and duty cycle measurement of pulse sequence period Instantaneous speed measurement Instantaneous frequency measurement Voltage measurement on an isolation boundary Distance/sonar measurement and scanning Flow measurement Capacitive touch application
Drive		
Pulse width modulation (PWM)/High-resolution pulse width modulation (HRPWM)	Up to 16 PWM channels It can generate high/low-side PWM with dead zones It supports such characteristics as valley switching (can switch PWM output at valley points) and blanking window	Flexible PWM waveform generation function, with excellent power topology coverage. The shadow dead zone and shadow action qualifier can achieve adaptive PWM generation and protection, thereby improving control accuracy and reducing power loss. It can improve power factor (PF) and total harmonic distortion (THD), and increase light load efficiency in the application of power factor correction (PFC).
	HRPWM functions: All 16 channels provide high-resolution functions (150ps); provide a step size of 150ps for duty cycle, period, dead zone, and phase offset, and improve the accuracy by 99%	It helps to precisely control and achieve better-performance high-frequency power conversion. It helps to achieve cleaner waveforms and avoid oscillation/period limitation at the output end.
	One-time and global reloading function	It is crucial for frequency conversion and multi-phase DC/DC applications to achieve high-frequency control loops (>2MHz). It can control interleaved LLC topology at high frequencies.
	It can perform independent PWM operation for cycle-by-cycle (CBC) trip events and one short trip (OST) events	It provides cycle-by-cycle protection and completely turns off PWM under fault conditions. It helps to achieve multi-phase PFC or DC/DC control.
	Load during SYNC (support of “shadow-to-activity” loading when a SYNC event occurs)	It supports frequency conversion applications (allowing LLC control in power conversion).
	PWM can be turned off without software intervention (without ISR delay)	It helps provide quick protection in the event of a fault
	Delayed tripping function	It helps to easily achieve dead zone using the peak current mode control (PCMC) phase-shifted full bridge (PSFB) C/DC converters, without consuming a large amount of CPU resources

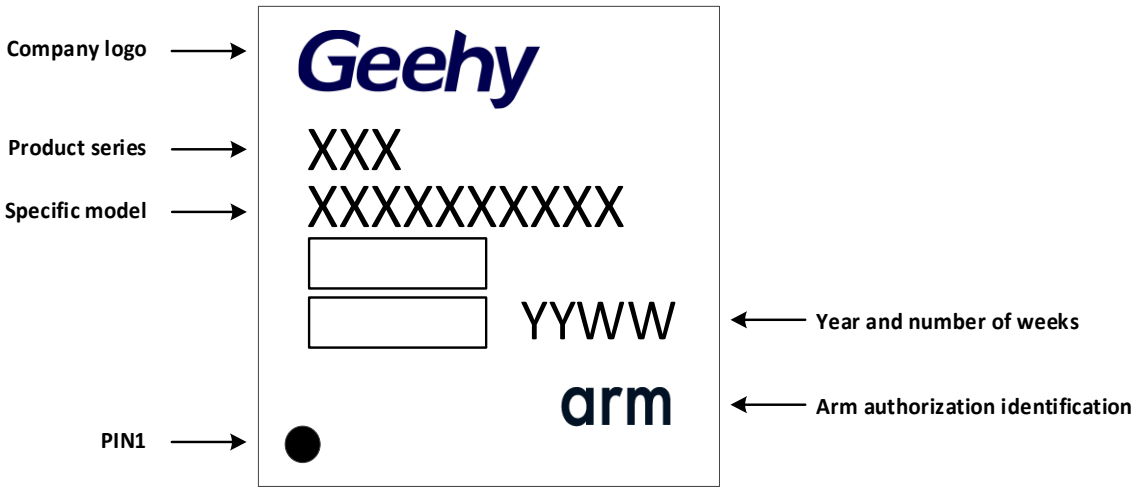
Module	Characteristics	System advantages
		(even in the event of trigger events based on comparator, trip, or synchronous input events).
	Dead band generator (DB) submodule	It can prevent the high and low-side gate electrodes from conducting simultaneously by adding programmable delays to the rising edge (RED) and falling edge (FED) of the PWM signals.
	Flexible PWM phase relationship and timer synchronization	Each PWM module can synchronize with other PWM modules or other peripherals. It can keep PWM edges synchronized with each other or with specific events. It supports flexible ADC scheduling using specific sampling windows, to maintain synchronization with power device switching.
Communication		
Serial peripheral interface (SPI)	2 high-speed SPI ports	It supports 25MHz
Serial communication interface (UART)	2 UART modules	Connect to the controller
Local interconnection network (LIN)	1 LIN	It provides a low-cost solution, which does not require the bandwidth and fault tolerance of controller area network (CAN). It can also serve as UART to communicate with other controllers.
Controller area network (CAN/DCAN)	1 DCAN module	Compatible with classic CAN modules
Internal integrated circuit (I2C)	1 I2C module	Connect to external EEPROM, sensors, or controllers
Power management bus (PMBus)	1 PMBus module Comply with SMI Forum PMBus specifications (Part I v1.0 and Part II v1.1)	Seamless host communication based on hardware
Quad serial peripheral interface（QSPI）	1 QSPI module	Connect to external Flash through single-wire, double-wire or four-wire SPI mode, so that when receiving serial data, the programmable delay of sampling time can achieve a higher data bit sampling ratio.
Other system characteristics		
Security enhancement function	Double-zone code security module (DCS) Watchdog Register write protection	**DCS:** Prevent replication and reverse engineering of proprietary codes **Watchdog:** If the CPU gets into an endless execution cycle, a reset will occur

Module	Characteristics	System advantages
	Lost clock detection logic (MCD) Error correction code (ECC) and parity check	**Register write protection:** Lock protection is provided for system configuration registers to prevent false CPU write **MCD:** Automatic clock fault detection **ECC and parity check:** Single-bit error correction and double-bit error detection
Crossbar switch (X-BAR)	It can flexibly connect to the device inputs, outputs, and internal resources in various configurations. Input X-BAR Output X-BAR PWM X-BAR FLB X-BAR	Enhance the universality of hardware design: **Input X-BAR:** Route signals from any GPIO to multiple IP blocks within the chip **Output X-BAR:** Route internal signals to designated GPIO pins **PWM X-BAR:** Route internal signals from various IP blocks to PWM **FLB X-BAR:** Allow users to transmit signals from various IP blocks to FLB

7. Package Information

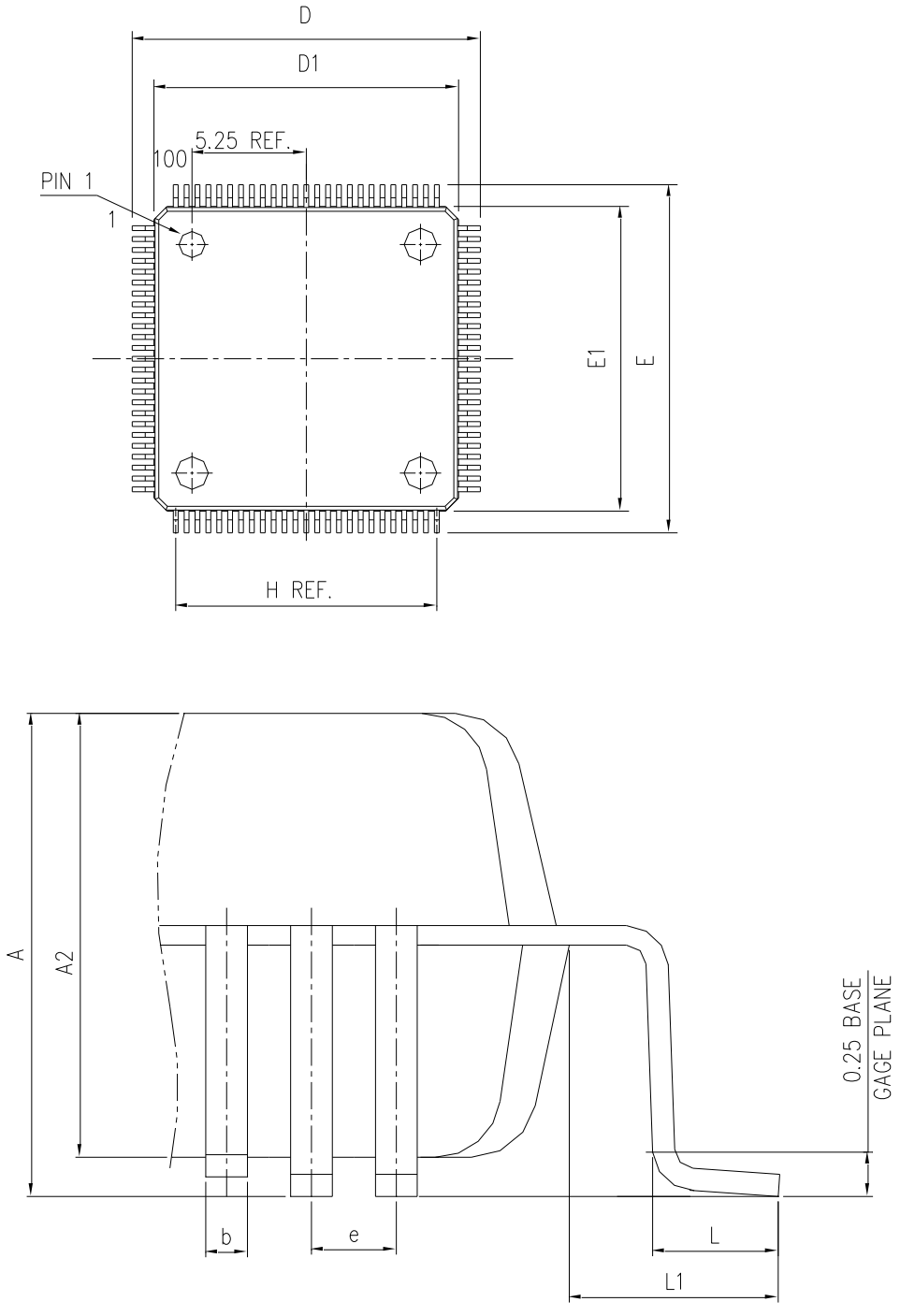
7.1. Product silk screen printing image

Figure 83 Product Silk Screen Printing Image (Example)



7.2. LQFP100 (14mm*14mm) package information

Figure 84LQFP100 Package Diagram



The figure is not drawn to scale.

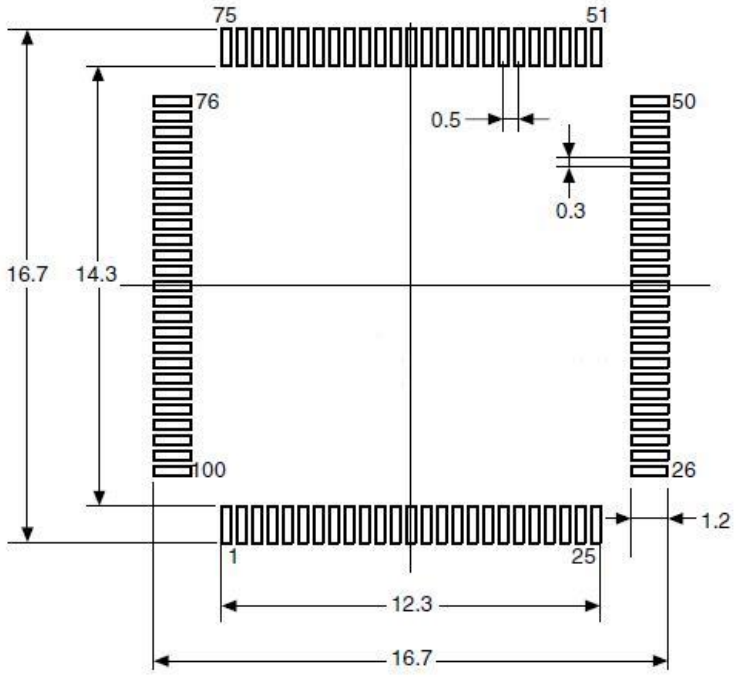
All pins should be soldered to the PCB.

Table 129 LQFP100 Package Data

DIMENSION LIST（FOOTPRINT: 2.00）			
S/N	**SYM**	**DIMENDIONS**	**REMARKS**
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	16.000±0.200	LEAD TIP TO TIP
4	D1	14.000±0.100	PKG LENGTH
5	E	16.000±0.200	LEAD TIP TO TIP
6	E1	14.000±0.100	PKG WDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H（REF）	（12.00）	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

Note: Dimensions are marked in millimeters.

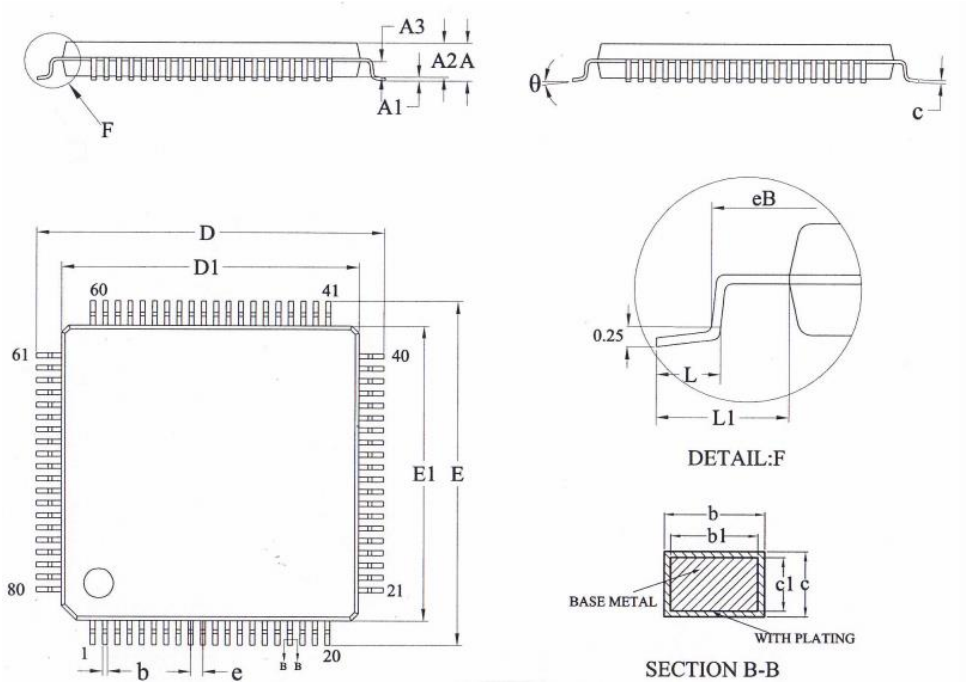
Figure 85 LQFP100, 14x14mm Welding Layout Recommendations



Note: Dimensions are marked in millimeters.

7.3. LQFP80 (12mm*12mm) package information

Figure 86 LQFP80 Package Diagram



The figure is not drawn to scale.

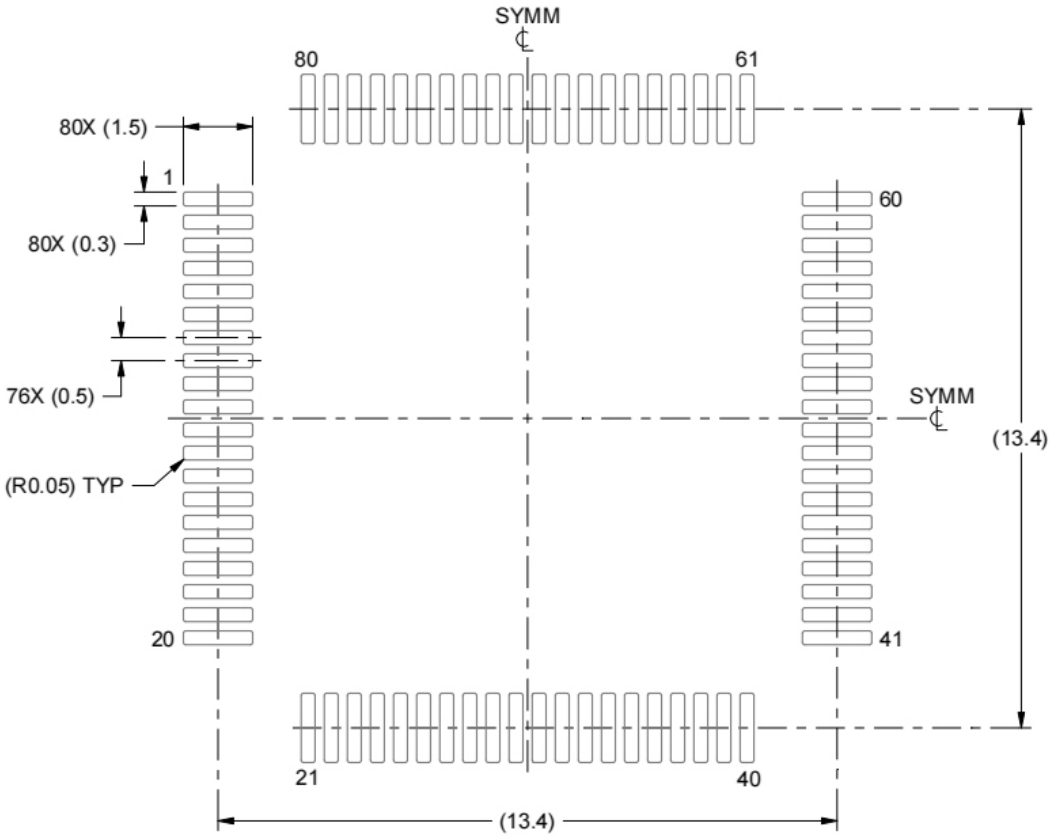
All pins should be soldered to the PCB.

Table 130 LQFP80 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
eB	13.05	—	13.25
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	—	7°

Note: Dimensions are marked in millimeters.

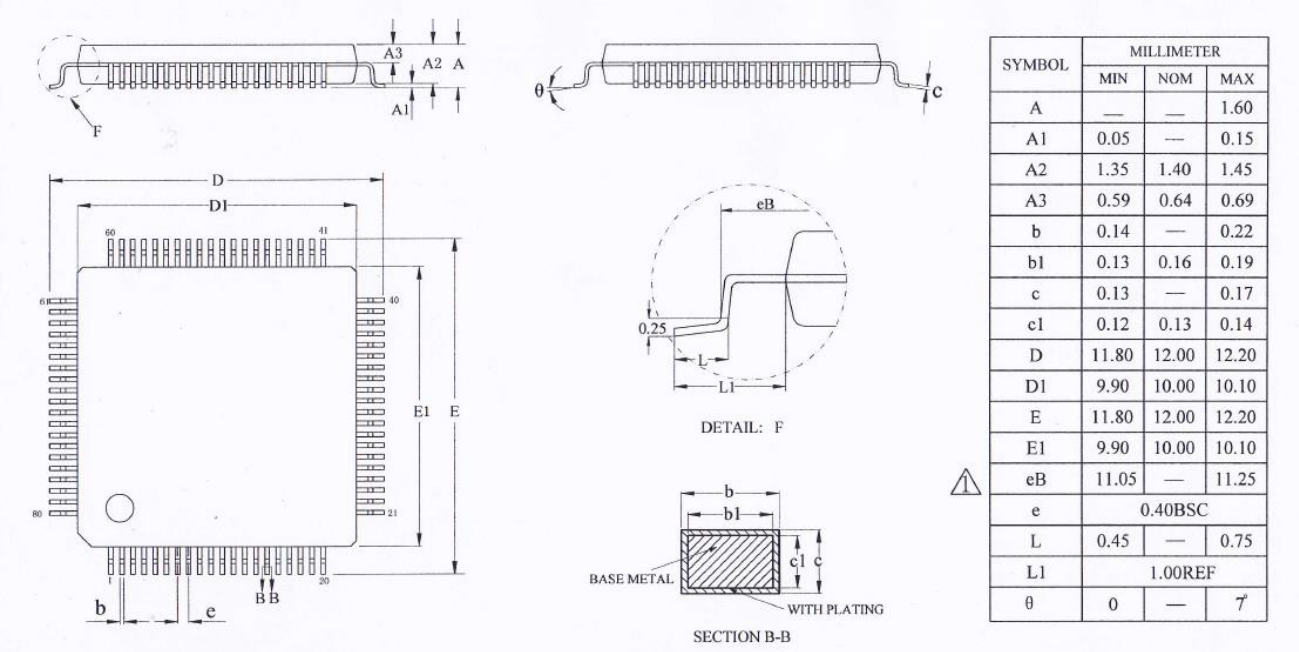
Figure 87 LQFP80, 12x12mm Welding Layout Recommendations



Note: Dimensions are marked in millimeters.

7.4. LQFP80 (10mm*10mm) package imformation

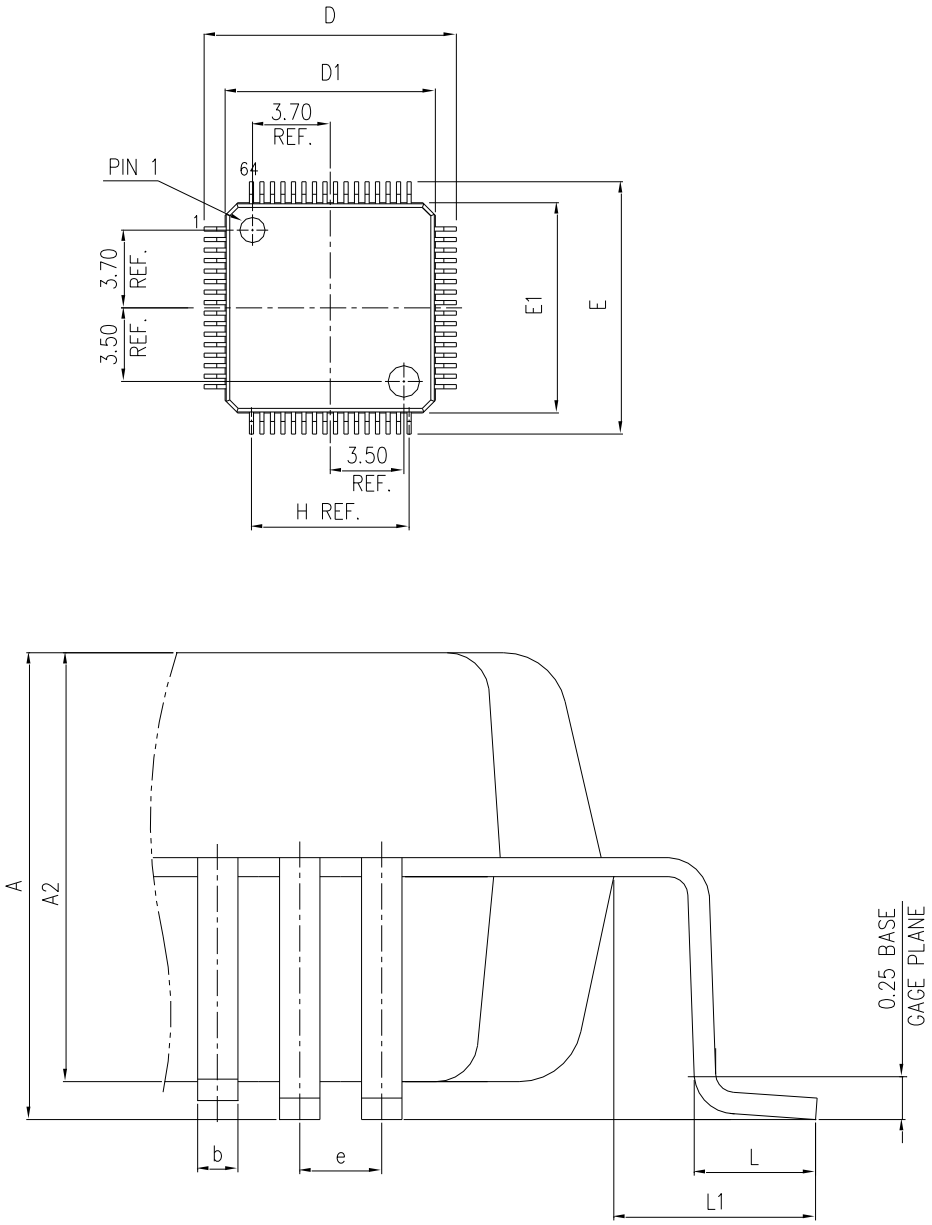
Figure 88 LQFP80 (10mm*10mm) package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.14	—	0.22
b1	0.13	0.16	0.19
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
eB	11.05	—	11.25
e	0.40BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

7.5. LQFP64 (10mm*10mm) package information

Figure 89 LQFP64 Package Diagram



The figure is not drawn to scale.

All pins should be soldered to the PCB.

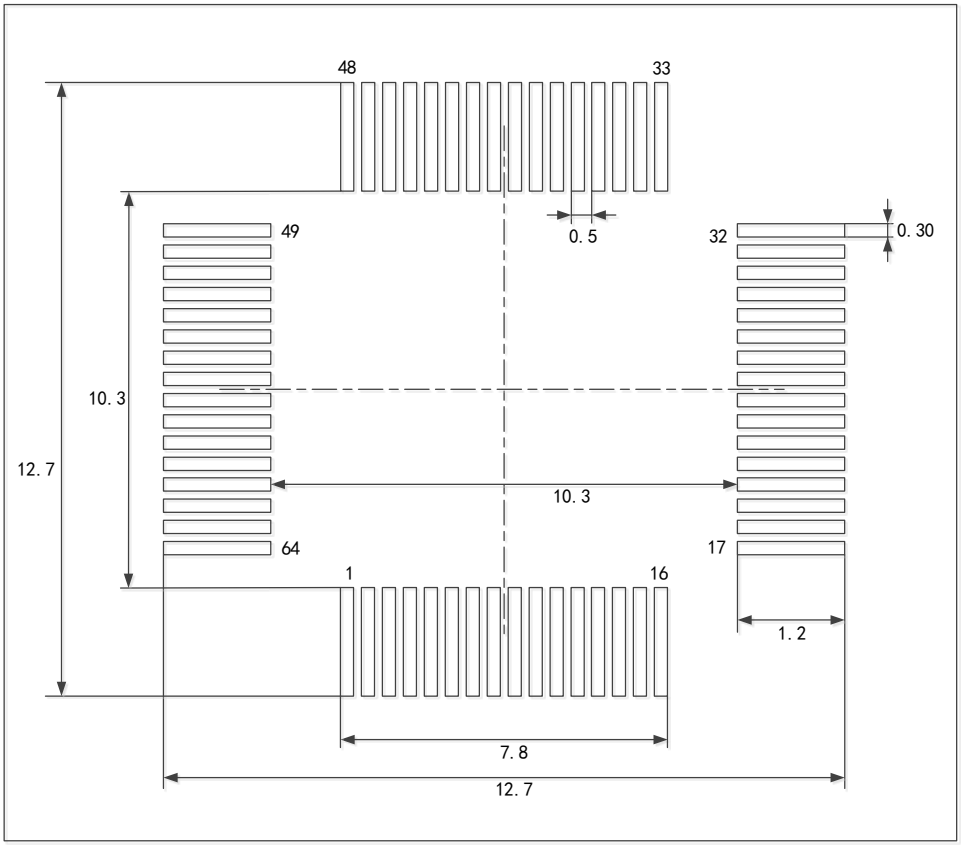
Table 131 LQFP64 Package Data

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.600	OVERALLHEIGHT

S/N	SYM	DIMENSIONS	REMARKS
2	A2	1.400±0.050	PKGTHICKNESS
3	D	12.000±0.200	LEADTIPTOTIP
4	D1	10.000±0.100	PKGLENGTH
5	E	12.000±0.200	LEADTIPTOTIP
6	E1	10.000±0.100	PKGWIDTH
7	L	0.600±0.150	FOOTLENGTH
8	L1	1.000REF.	LEADLENGTH
9	e	0.500BASE	LEADPITCH
10	H (REF)	(7.500)	GUM.LEADPITCH
11	b	0.220±0.050	LEADWIDTH

Note: Dimensions are marked in millimeters.

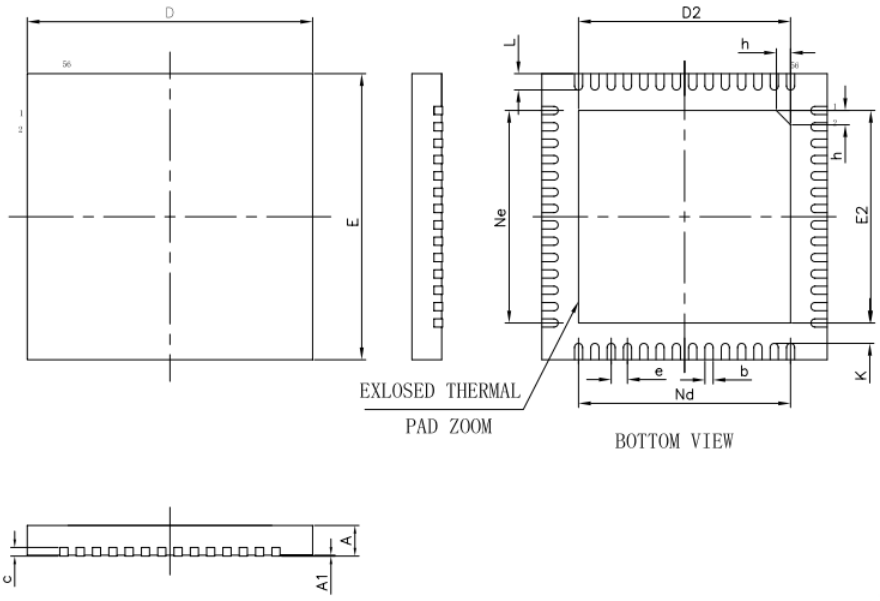
Figure 90 LQFP64, 10x10 Welding Layout Recommendations



Note: Dimensions are marked in millimeters.

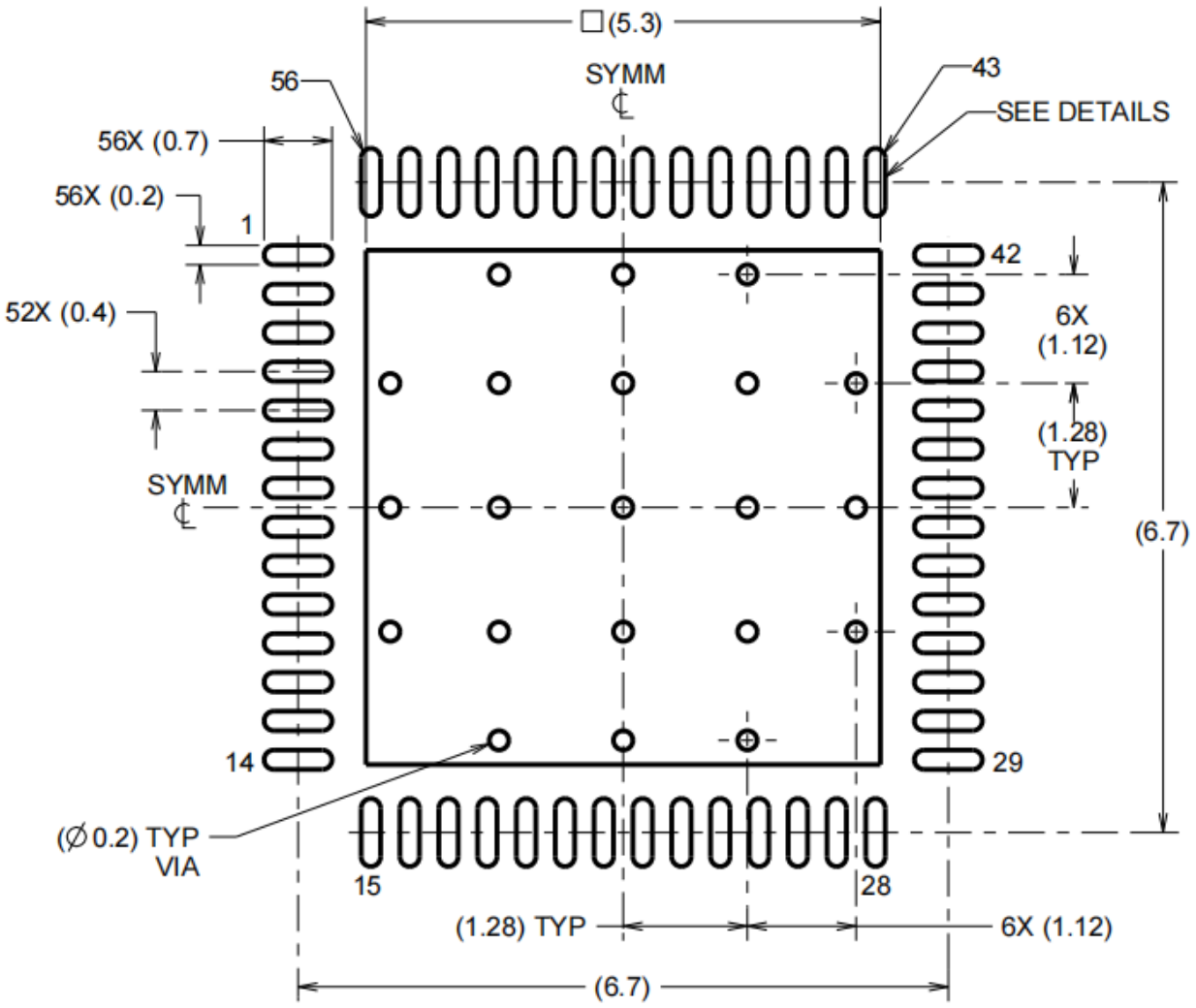
7.6. QFN56 (7mm*7mm) package information

Figure 91 QFN56 Package Diagram



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	6.90	7.00	7.10
D2	5.10	5.20	5.30
e	0.40BSC		
Nd	5.20BSC		
Ne	5.20BSC		
E	6.90	7.00	7.10
E2	5.10	5.20	5.30
K	0.20	—	—
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	217*217		

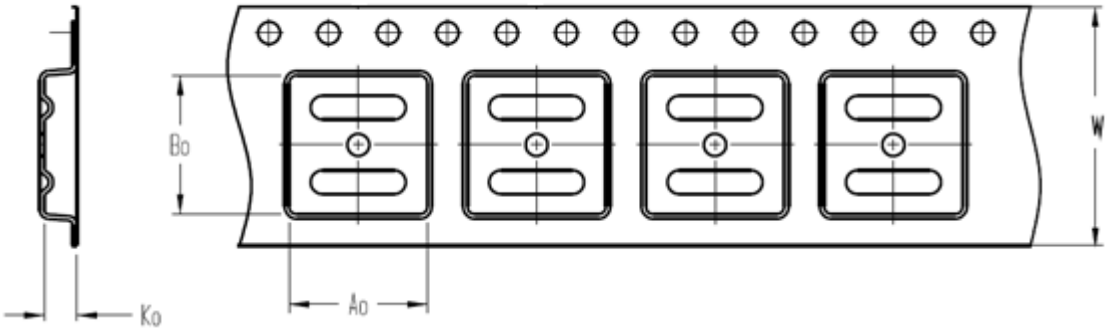
Figure 92 QFN56, 7x7mm Welding Recommendations



8. Packaging Information

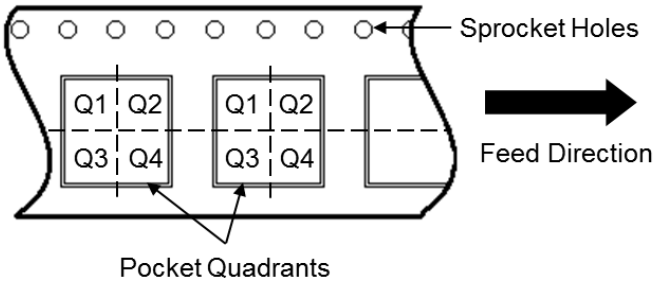
8.1. Reel packaging

Figure 93 Reel Packaging Specification Drawing

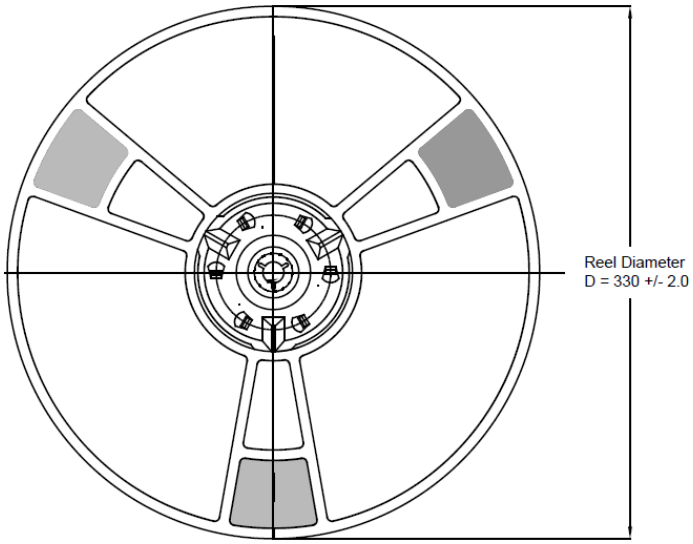


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions



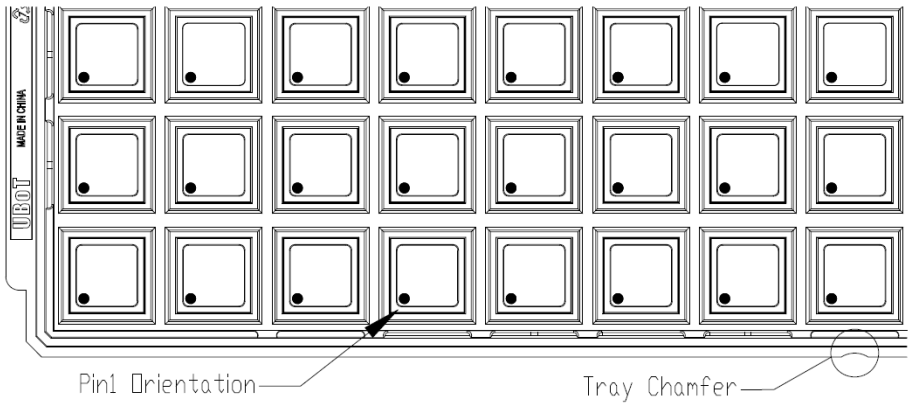
All photos are for reference only, and the appearance is subject to the product.

Table 132 Parameter Specification Table of Reel Packaging

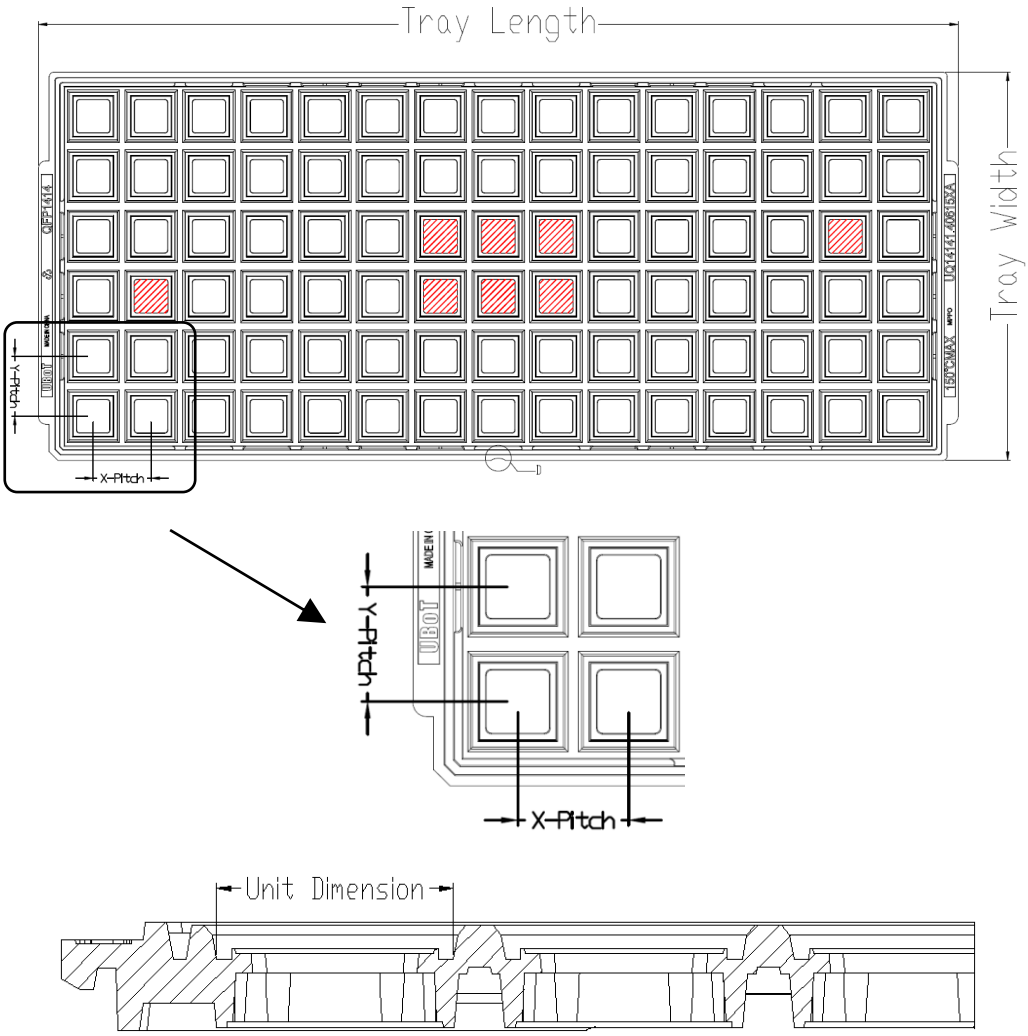
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
G32R501DRYT7	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
G32R501RYT7	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
G32R501RCT7	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
G32R501DRCT7	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
G32R501DRYT8Q	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1

8.2. Pallet packaging

Figure 94 Pallet Packaging Diagram



Tray Dimensions



All photos are for reference only, and the appearance is subject to the product

Table 133 Parameter Specification Table of Pallet Packaging

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
G32R501DVYT7	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
G32R501DMYT7	LQFP	80	1190	14.8	14.8	17.9	18	322.6	135.9
G32R501DPYT7	LQFP	80	1600	12.3	12.3	15.2	15.7	322.6	135.9
G32R501DRYT7	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
G32R501DNYU7	QFN	56	2500	9.7	9.7	12.2	12.6	322.6	135.9
G32R501VYT7	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
G32R501MYT7	LQFP	80	1190	14.8	14.8	17.9	18	322.6	135.9
G32R501RYT7	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
G32R501NYU7	QFN	56	2500	9.7	9.7	12.2	12.6	322.6	135.9

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
G32R501VCT7	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
G32R501MCT7	LQFP	80	1190	14.8	14.8	17.9	18	322.6	135.9
G32R501RCT7	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
G32R501NCU7	QFN	56	2500	9.7	9.7	12.2	12.6	322.6	135.9
G32R501DVCT7	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
G32R501DMCT7	LQFP	80	1190	14.8	14.8	17.9	18	322.6	135.9
G32R501DRCT7	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
G32R501DNCU7	QFN	56	2500	9.7	9.7	12.2	12.6	322.6	135.9
G32R501DVYT8Q	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
G32R501DMYT8Q	LQFP	80	1190	14.8	14.8	17.9	18	322.6	135.9
G32R501DRYT8Q	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
G32R501DNYU8	QFN	56	2500	9.7	9.7	12.2	12.6	322.6	135.9

9. Ordering Information

Figure 95 G32R501 Series Ordering Information

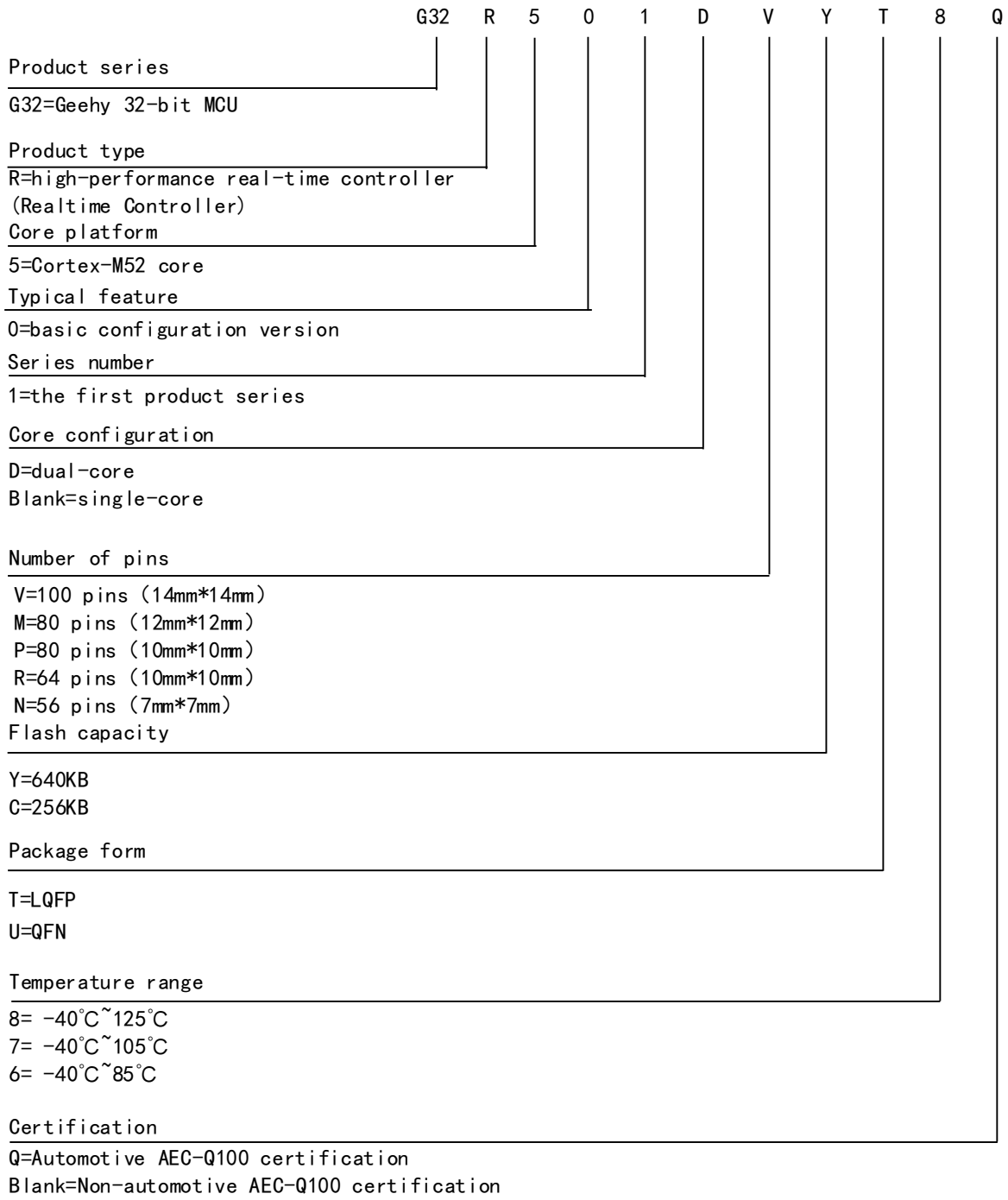


Table 134 Ordering Information List

Order Code	FLASH（KB）	SRAM（KB）	Package	Packaging	SPQ	Temperature range
G32R501DVYT7	640	128	LQFP100	Pallet	900	Industrial grade -40℃~105℃
G32R501DMYT7	640	128	LQFP80	Pallet	1190	Industrial grade -40℃~105℃
G32R501DPYT7	640	128	LQFP80 (10mm*10mm)	Pallet	1600	Industrial grade -40℃~105℃
G32R501DRYT7	640	128	LQFP64	Pallet	1600	Industrial grade -40℃~105℃
G32R501DRYT7	640	128	LQFP64	Reel	1000	Industrial grade -40℃~105℃
G32R501DNYU7	640	128	QFN56	Pallet	2500	Industrial grade -40℃~105℃
G32R501VYT7	640	128	LQFP100	Pallet	900	Industrial grade -40℃~105℃
G32R501MYT7	640	128	LQFP80	Pallet	1190	Industrial grade -40℃~105℃
G32R501RYT7	640	128	LQFP64	Pallet	1600	Industrial grade -40℃~105℃
G32R501RYT7	640	128	LQFP64	Reel	1000	Industrial grade -40℃~105℃
G32R501NYU7	640	128	QFN56	Pallet	2500	Industrial grade -40℃~105℃
G32R501VCT7	256	128	LQFP100	Pallet	900	Industrial grade -40℃~105℃
G32R501MCT7	256	128	LQFP80	Pallet	1190	Industrial grade -40℃~105℃
G32R501RCT7	256	128	LQFP64	Pallet	1600	Industrial grade -40℃~105℃
G32R501RCT7	256	128	LQFP64	Reel	1000	Industrial grade -40℃~105℃
G32R501NCU7	256	128	QFN56	Pallet	2500	Industrial grade -40℃~105℃
G32R501DVCT7	256	128	LQFP100	Pallet	900	Industrial grade -40℃~105℃
G32R501DMCT7	256	128	LQFP80	Pallet	1190	Industrial grade -40℃~105℃
G32R501DRCT7	256	128	LQFP64	Pallet	1600	Industrial grade -40℃~105℃
G32R501DRCT7	256	128	LQFP64	Reel	1000	Industrial grade -40℃~105℃
G32R501DNCU7	256	128	QFN56	Pallet	2500	Industrial grade -40℃~105℃
G32R501DVYT8Q	640	128	LQFP100	Pallet	900	Automatic grade -40℃~125℃
G32R501DMYT8Q	640	128	LQFP80	Pallet	1190	Automatic grade -40℃~125℃
G32R501DRYT8Q	640	128	LQFP64	Pallet	1600	Automatic grade -40℃~125℃
G32R501DRYT8Q	640	128	LQFP64	Reel	1000	Automatic grade -40℃~125℃
G32R501DNYU8	640	128	QFN56	Pallet	2500	Industrial grade -40℃~125℃

Note: The automotive grade model (G32R501DxYx8Q) is currently in the trial production stage and is scheduled for mass production and supply in Q4 2025. The specific time will be based on official notifications from Geehy.

10. Commonly Used Modules and Abbreviations

Table 135 Commonly Used Function Module Denomination

Full name	Abbreviation
Floating Point Unit	FPU
Trigonometric Math Unit	TMU
Viterbi, Complex Math and CRC Unit	VCU
Nested Vector Interrupt Controller	NVIC
External Interrupt	EXTI
General-purpose IO	GPIO
Watchdog Timer	WDT
Timer	TMR
CRC Controller	CRC
Power Management Bus	PMBus
DMA controller	DMA
Analog-to-digital converter	ADC
Digital-to-analog converter	DAC
Comparator Subsystem	COMP
Real-time Clock	RTC
Controller Area Network	CAN
Inter-integrated circuit	I2C
Serial Peripheral Interface	SPI
Universal Asynchronous Receiver/Transmitter	UART
Local Interconnection Network	LIN
Quad serial peripheral interface	QSPI
Crossbar switch	X-BAR
Math Instruction Extension	Zidian

11. Revision history

Table 136 Document Revision History

Date	Version	Revision History
January 2025	1.0	New
February 2025	1.1	(1) Update the pin information for the LQFP80 package. (2) Update the ordering information for the QFN56 package. (3) Correct the typographical error in the product information table for the package.
March 2025	1.2	(1) Remove the -40~85℃ condition from section 5.3. (2) Revise the schematic diagram of the simulation subsystem. (3) Revise the product silkscreen diagram. (4) Revise the description of the boot mode. (5) Add a description of the chip dimensions in the product characteristics section. (6) Revise the description of DAC reference voltage. (7) Revise the number of COMP in Product Information Table
May 2025	1.3	(1) Correction of Boot mode pin number (2) Correction of the internal oscillator name for the zero pin in the product information table (3) Update of CFGSMS logic block description (4) Update of the format for the LQFP80 pin diagram (5) Update of the product model information for G32R501DPYT7
May 2025	1.4	(1) Correction Table5 Digital Signals

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